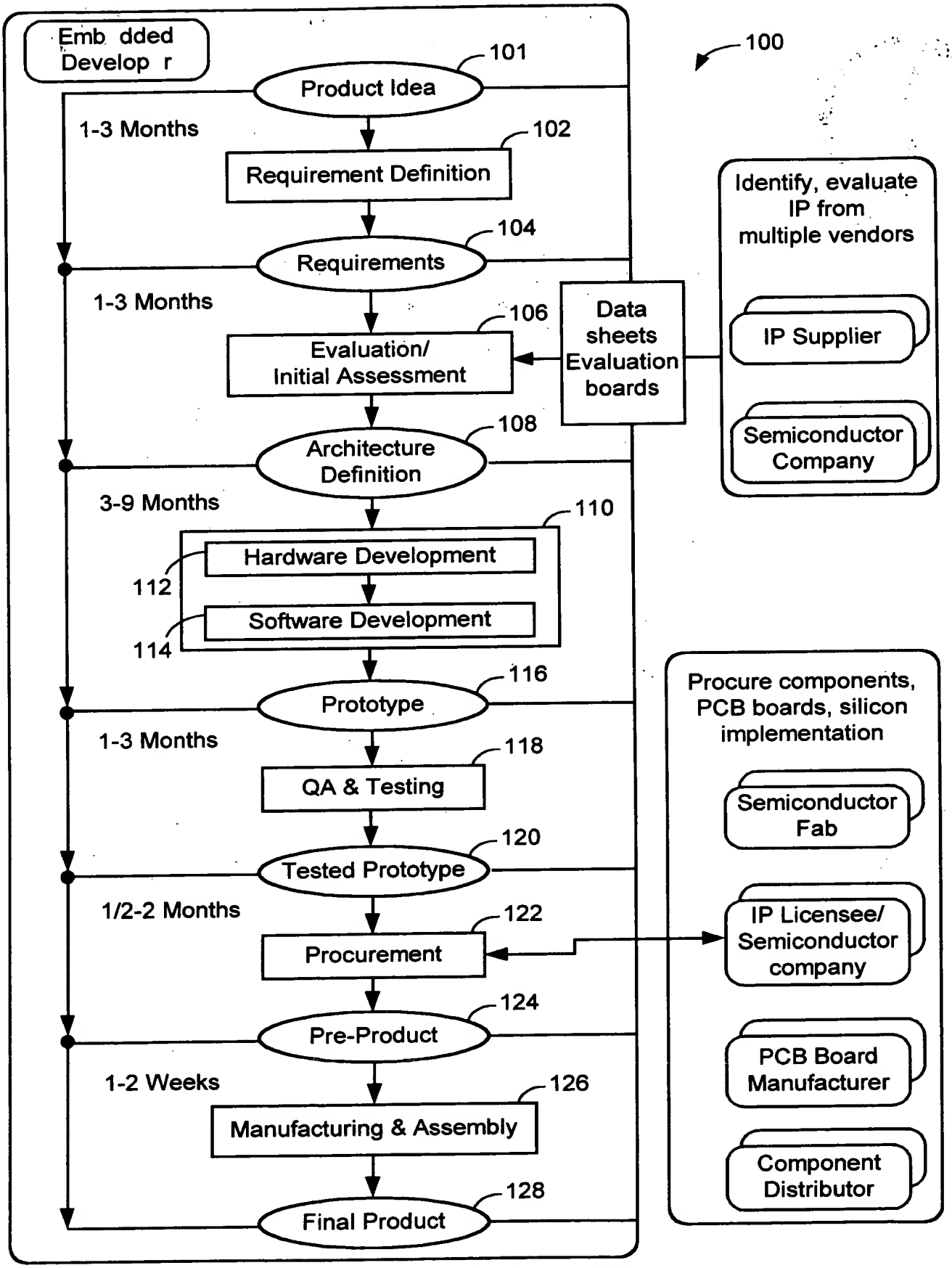
#4



Figur 1 (Prior Art)

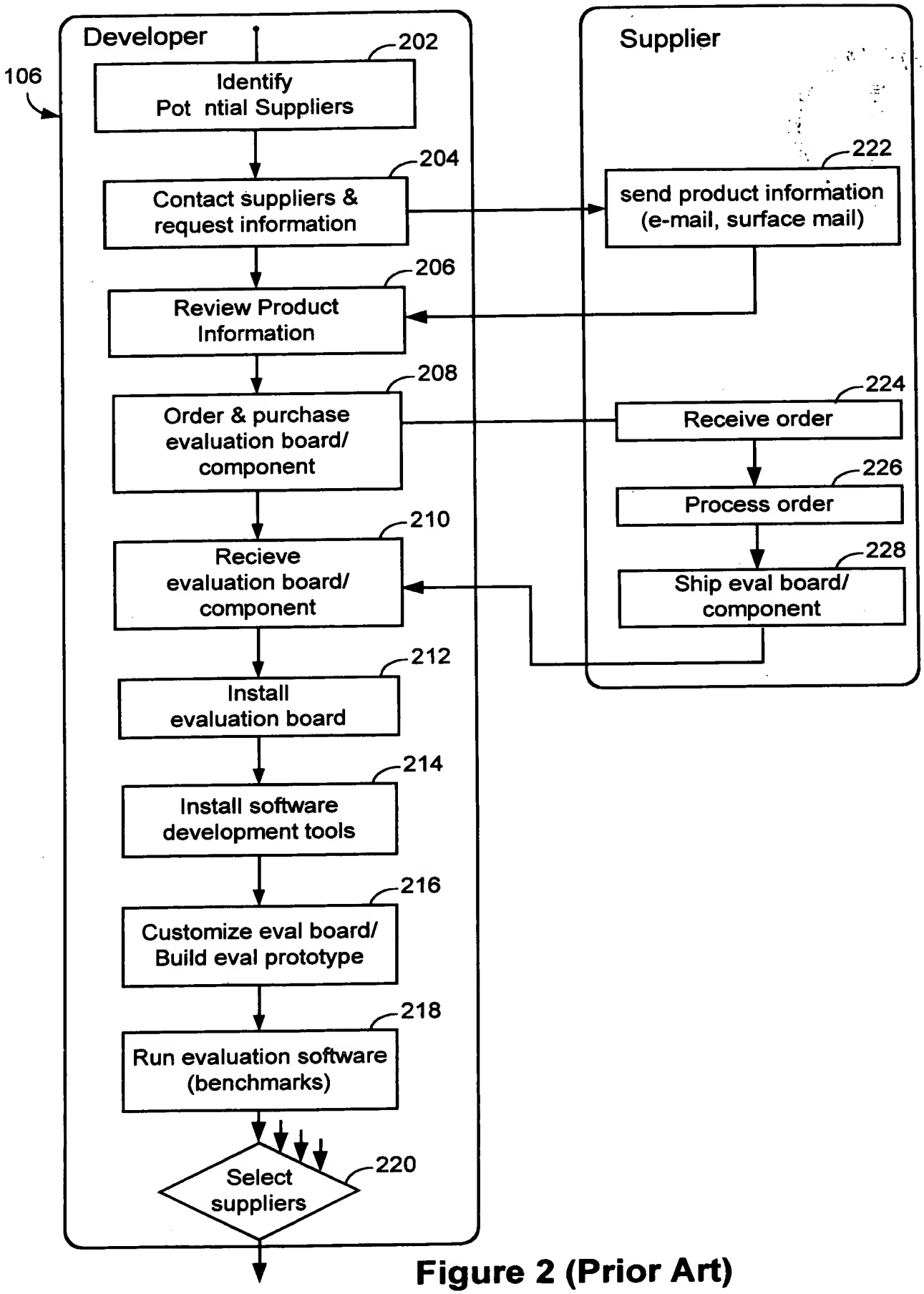
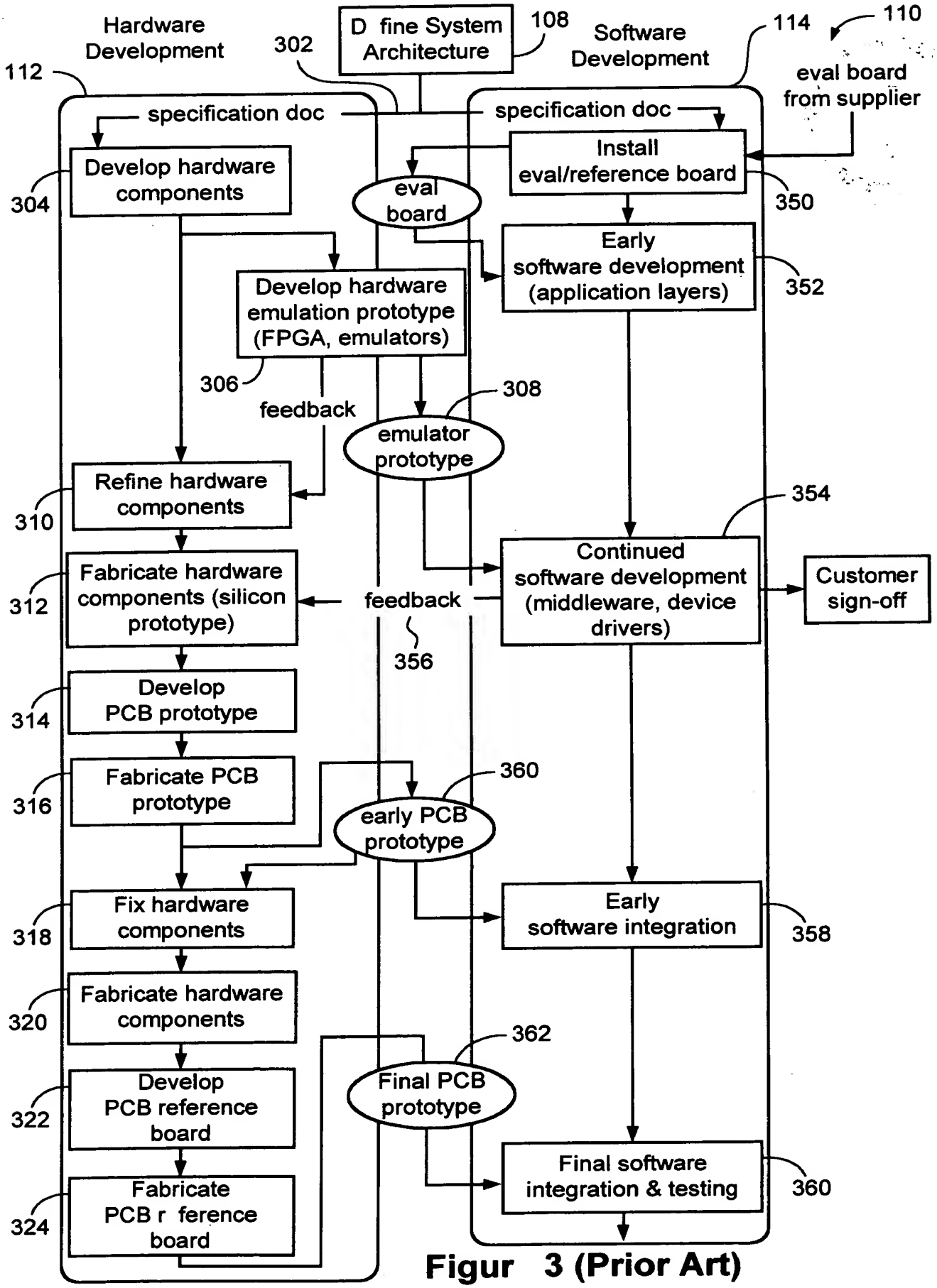


Figure 2 (Prior Art)



Figur 3 (Prior Art)

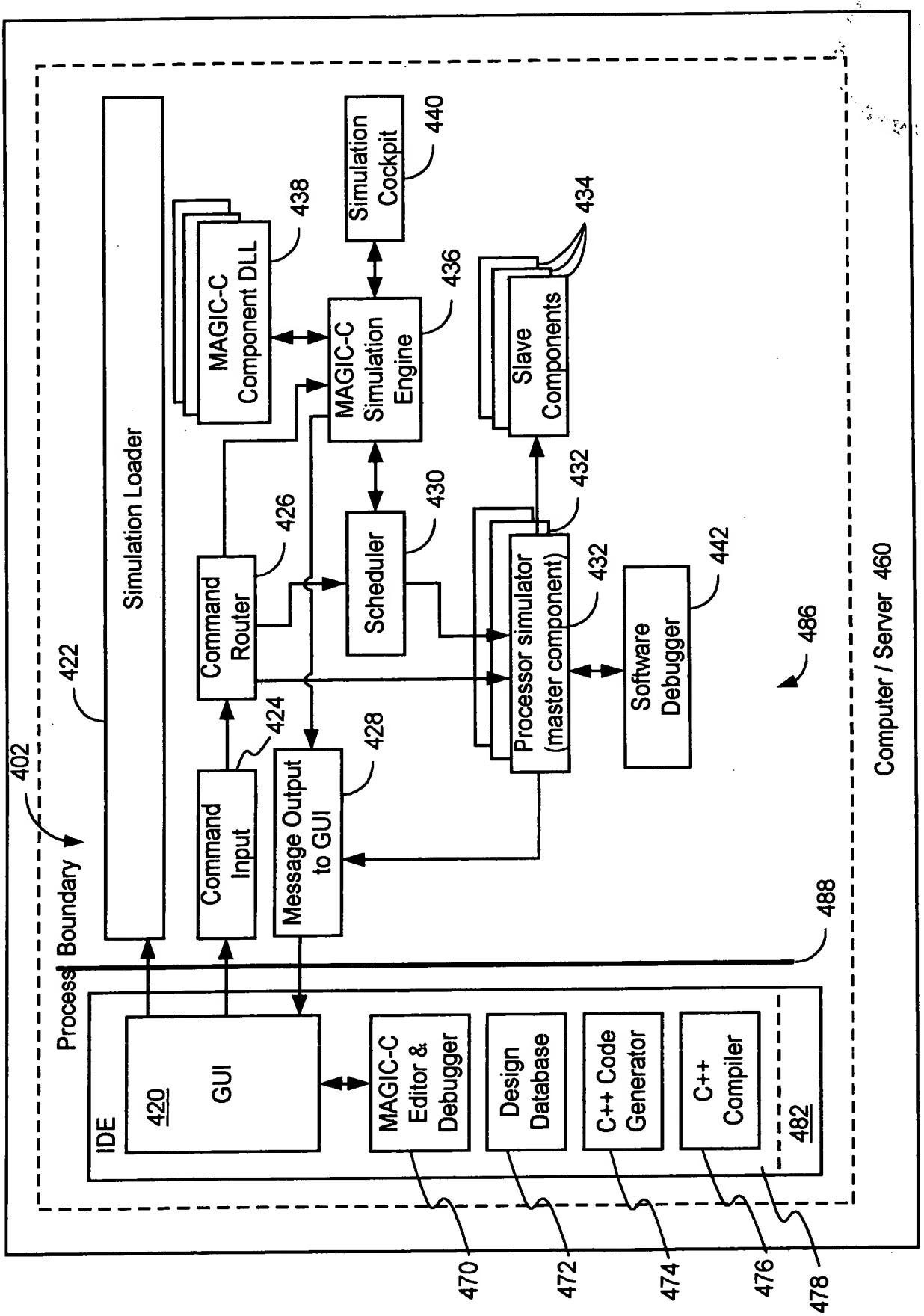

Computer / Server 460
Process Boundary
402
IDE
420
GUI
Simulation Loader
422
Command Input
424
Command Router
426
Message Output to GUI
428
Scheduler
430
Processor simulator (master component)
432
Slave Components
434
MAGIC-C Simulation Engine
436
MAGIC-C Component DLL
438
Simulation Cockpit
440
Software Debugger
442
486
488
MAGIC-C Editor & Debugger
Design Database
C++ Code Generator
C++ Compiler
482
470
472
474
476
478

Figure 4A

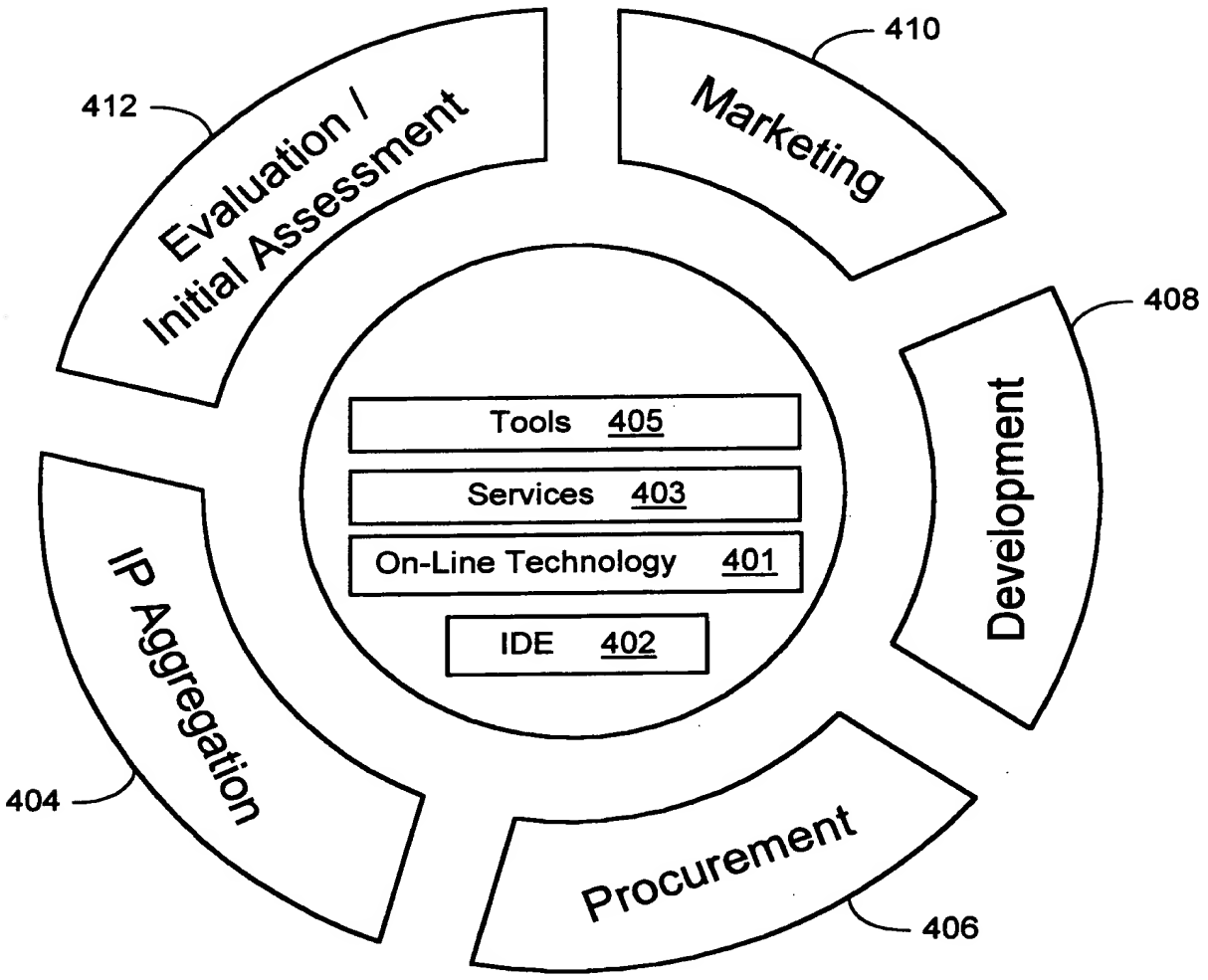
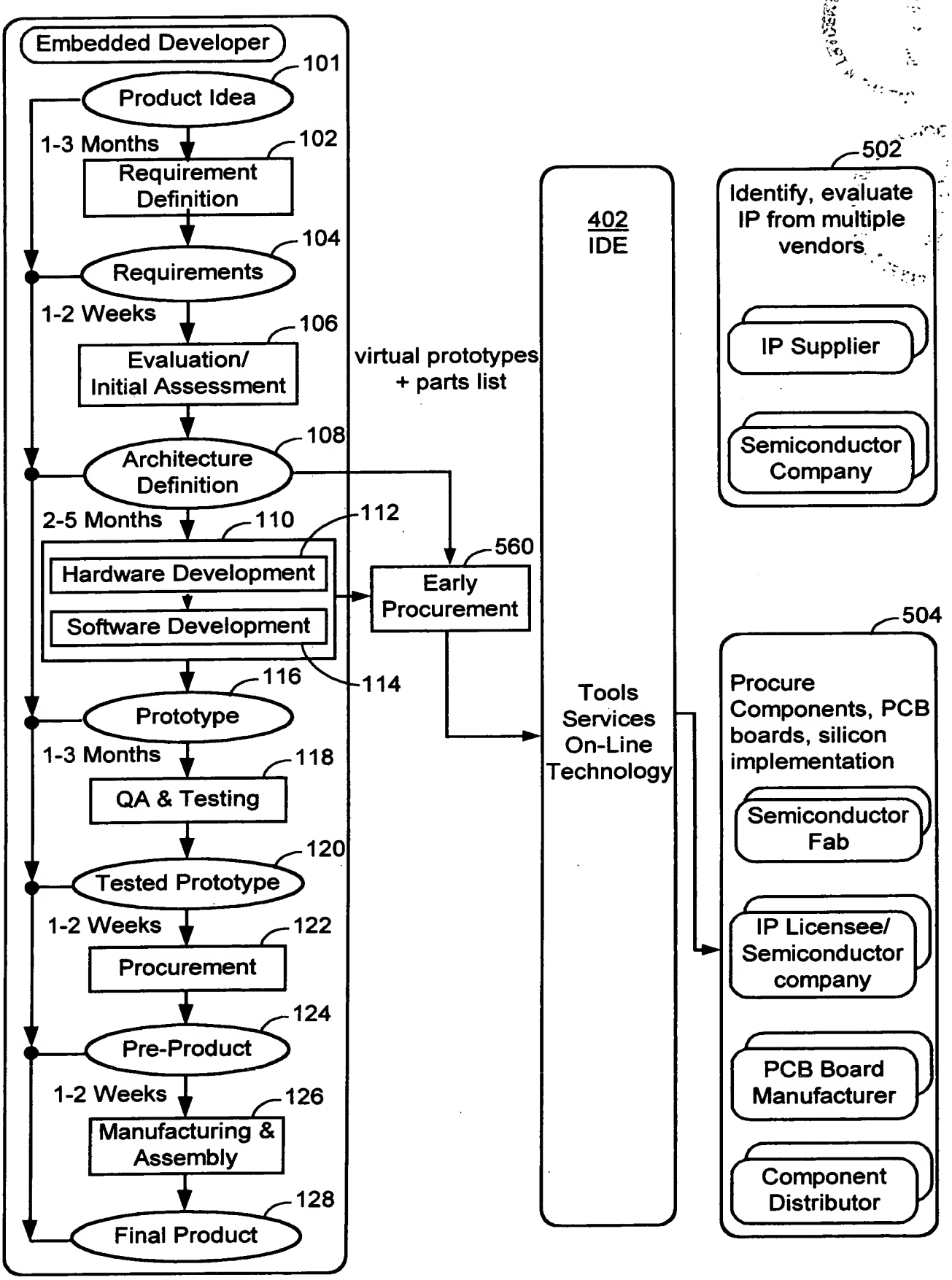
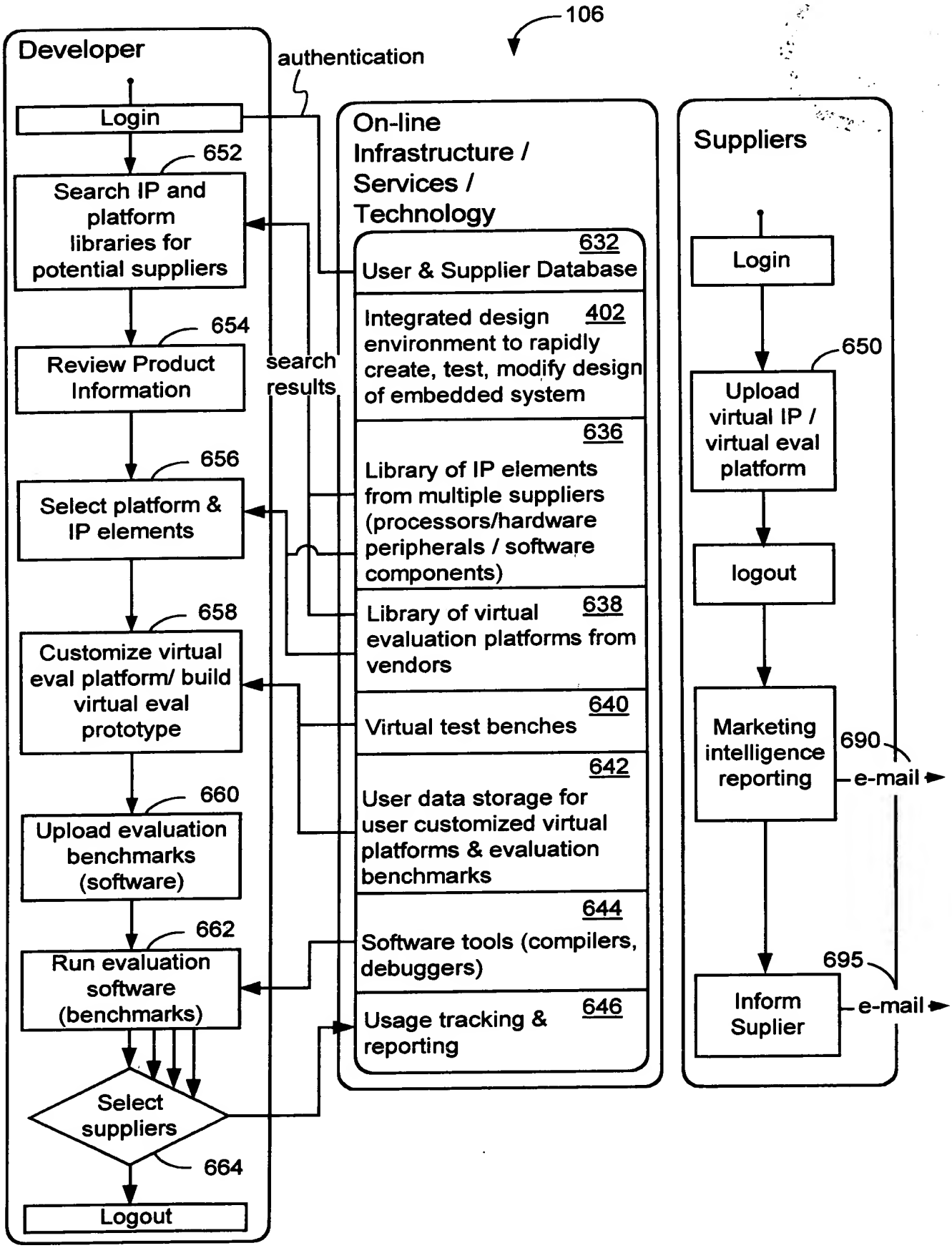

412
Evaluation / Initial Assessment
410
Marketing
408
Development
406
Procurement
404
IP Aggregation
Tools 405
Services 403
On-Line Technology 401
IDE 402

Figure 4B


Embedded Developer
101
Product Idea
1-3 Months
102
Requirement Definition
104
Requirements
1-2 Weeks
106
Evaluation/ Initial Assessment
108
Architecture Definition
2-5 Months
110
112
Hardware Development
Software Development
114
116
Prototype
1-3 Months
118
QA & Testing
120
Tested Prototype
1-2 Weeks
122
Procurement
124
Pre-Product
1-2 Weeks
126
Manufacturing & Assembly
128
Final Product
virtual prototypes + parts list
560
Early Procurement
402
IDE
Tools
Services
On-Line
Technology
502
Identify, evaluate IP from multiple vendors
IP Supplier
Semiconductor Company
504
Procure Components, PCB boards, silicon implementation
Semiconductor Fab
IP Licensee/ Semiconductor company
PCB Board Manufacturer
Component Distributor

Figur 5


106
Developer
authentication
Login
652
Search IP and platform libraries for potential suppliers
654
Review Product Information
656
Select platform & IP elements
658
Customize virtual eval platform/ build virtual eval prototype
660
Upload evaluation benchmarks (software)
662
Run evaluation software (benchmarks)
Select suppliers
664
Logout
search results
On-line Infrastructure / Services / Technology
632
User & Supplier Database
Integrated design environment to rapidly create, test, modify design of embedded system 402
636
Library of IP elements from multiple suppliers (processors/hardware peripherals / software components)
Library of virtual evaluation platforms from vendors 638
640
Virtual test benches
642
User data storage for user customized virtual platforms & evaluation benchmarks
644
Software tools (compilers, debuggers)
Usage tracking & reporting 646
Suppliers
Login
650
Upload virtual IP / virtual eval platform
logout
Marketing intelligence reporting
690
e-mail
695
Inform Suplier
e-mail

Figur 6

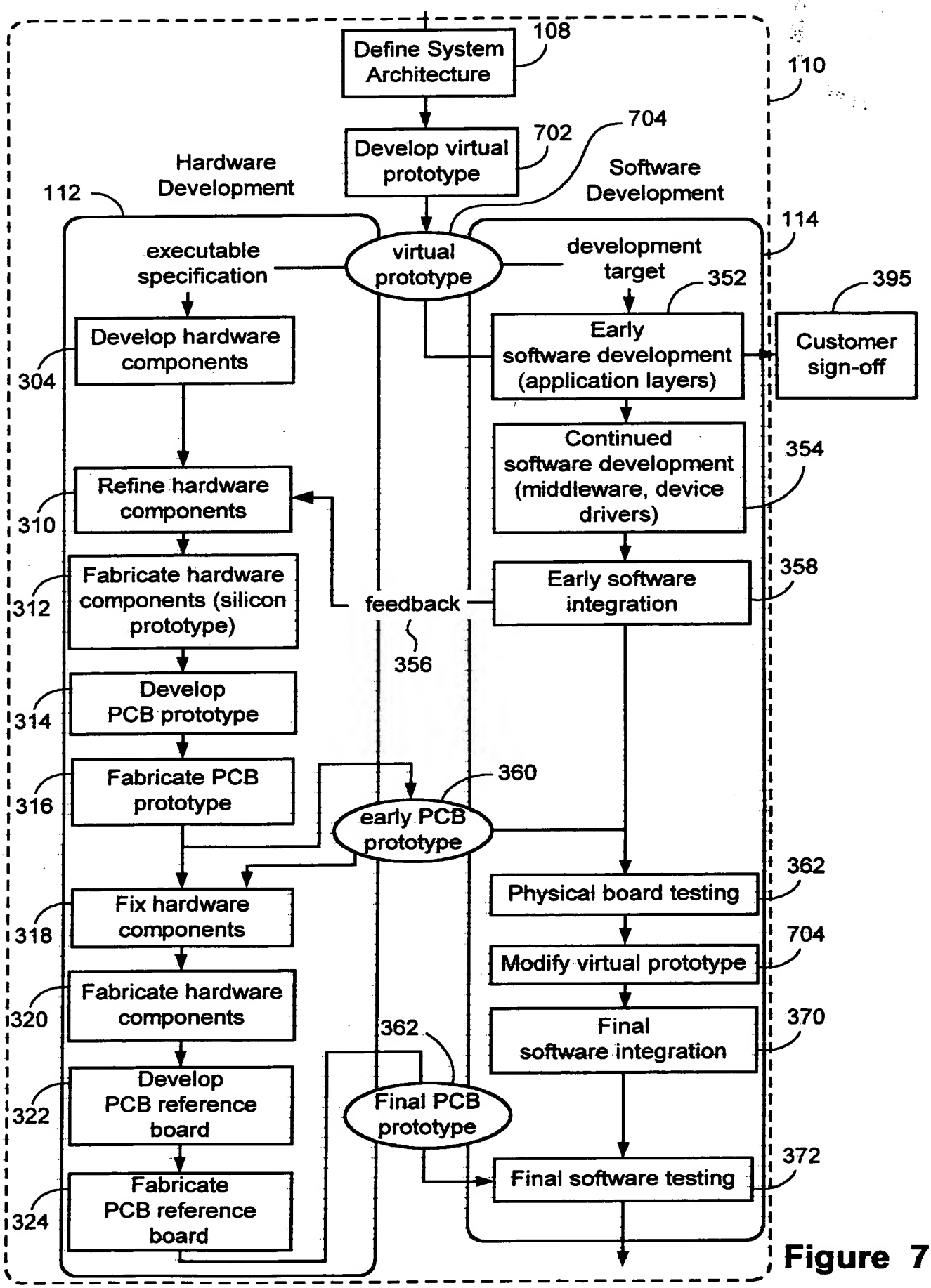

Define System Architecture
108
110
Develop virtual prototype
702
704
Hardware Development
Software Development
112
114
executable specification
virtual prototype
development target
352
395
Develop hardware components
304
Early software development (application layers)
Customer sign-off
Continued software development (middleware, device drivers)
354
Refine hardware components
310
Fabricate hardware components (silicon prototype)
312
feedback
356
Early software integration
358
Develop PCB prototype
314
Fabricate PCB prototype
316
360
early PCB prototype
Physical board testing
362
Fix hardware components
318
Modify virtual prototype
704
Fabricate hardware components
320
Final software integration
370
362
Develop PCB reference board
322
Final PCB prototype
Final software testing
372
Fabricate PCB reference board
324

Figure 7

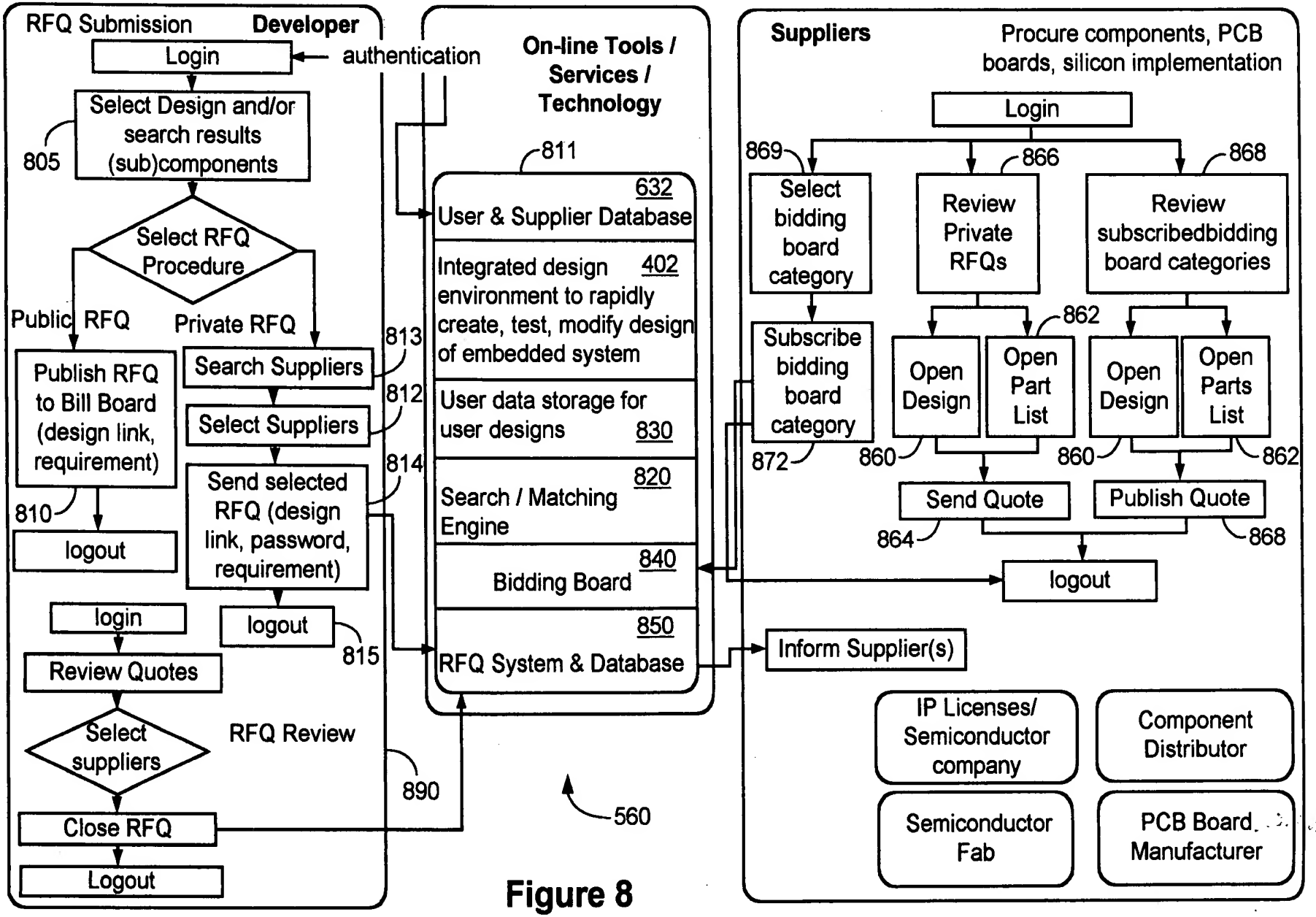


Figure 8

Application No. 09/872,435
Title: METHOD AND SYSTEM FOR VIRTUAL PROTOTYPING
Inventor(s): Stephen L. Bade et al.
Atty. Docket No.: 22178-05012
Sheet 9 of 65

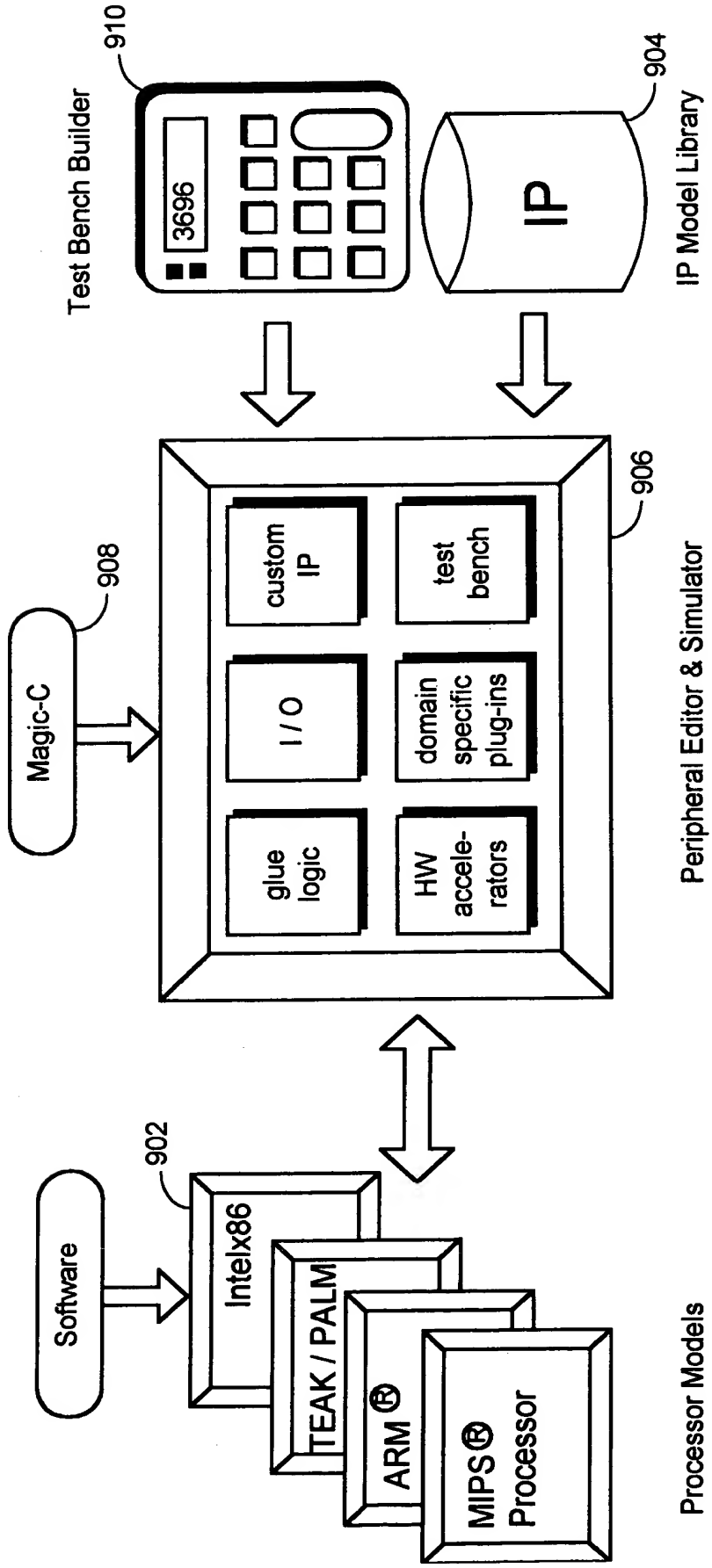
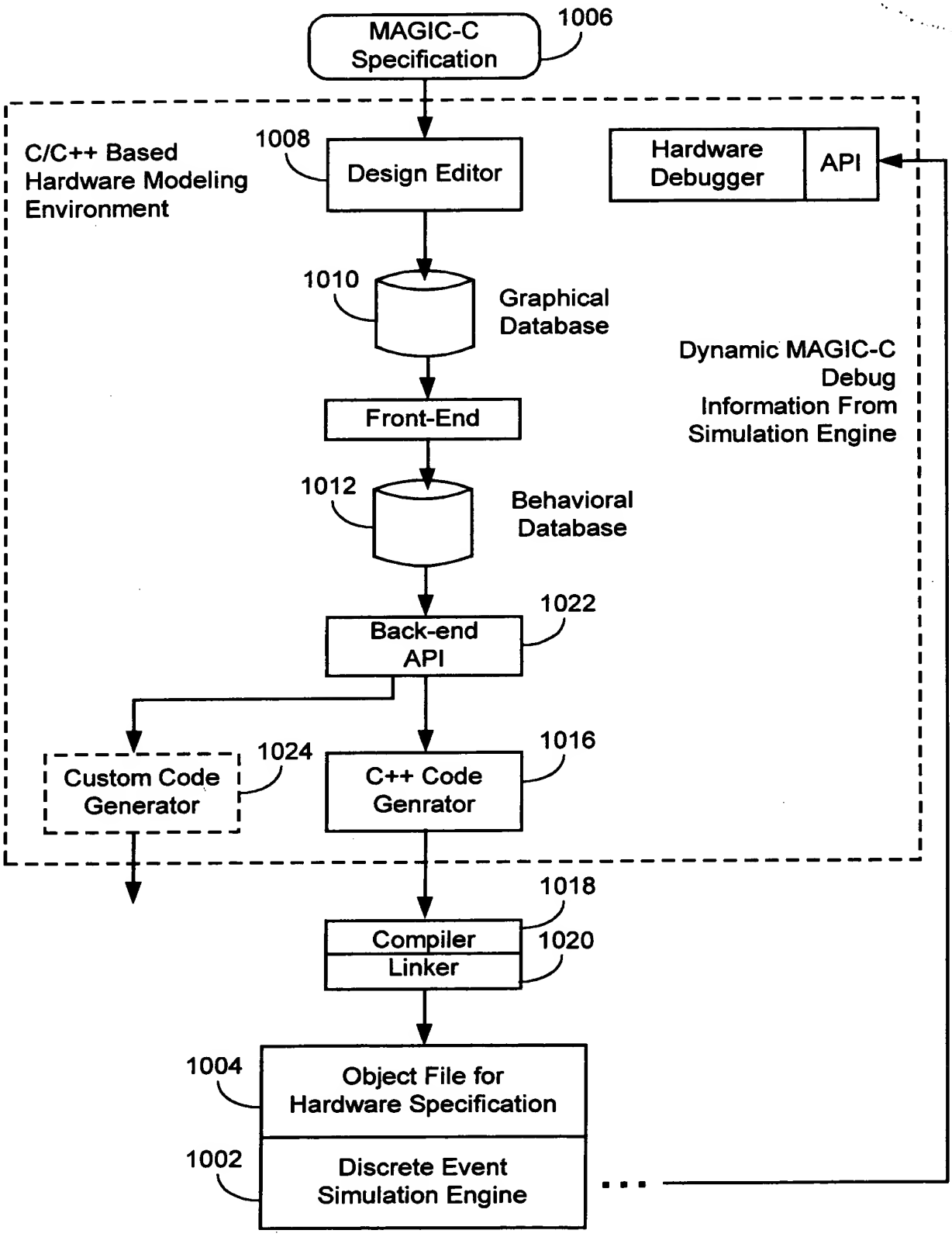

910
Test Bench Builder
3696
904
IP
IP Model Library
906
custom IP
test bench
I / O
domain specific plug-ins
glue logic
HW accele-rators
Peripheral Editor & Simulator
908
Magic-C
902
Software
IntelX86
TEAK / PALM
ARM®
MIPS® Processor
Processor Models

Figure 9


MAGIC-C Specification
1006
C/C++ Based Hardware Modeling Environment
1008
Design Editor
Hardware Debugger
API
1010
Graphical Database
Dynamic MAGIC-C Debug Information From Simulation Engine
Front-End
1012
Behavioral Database
1022
Back-end API
1024
Custom Code Generator
1016
C++ Code Genrator
1018
Compiler
1020
Linker
1004
Object File for Hardware Specification
1002
Discrete Event Simulation Engine

Figur 10

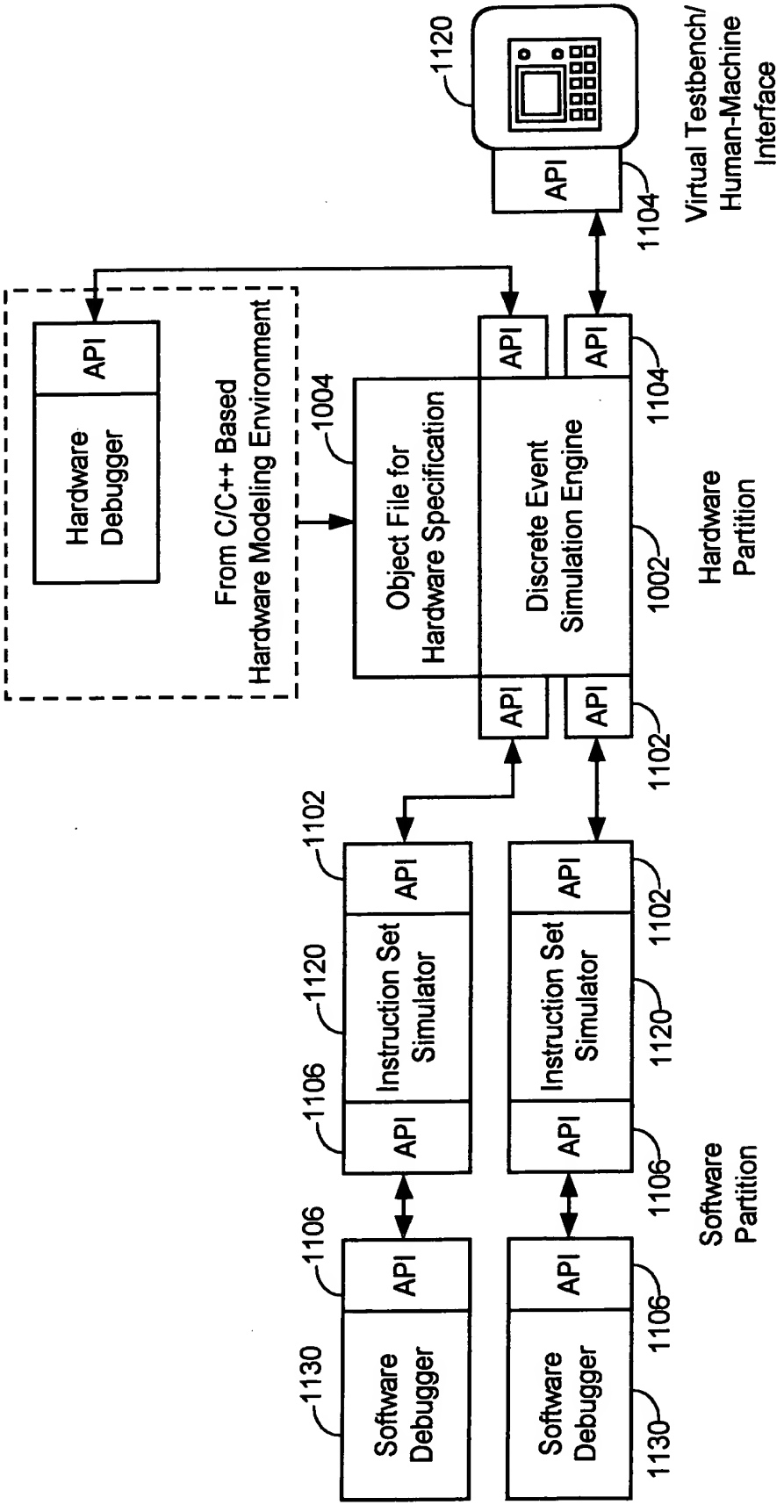
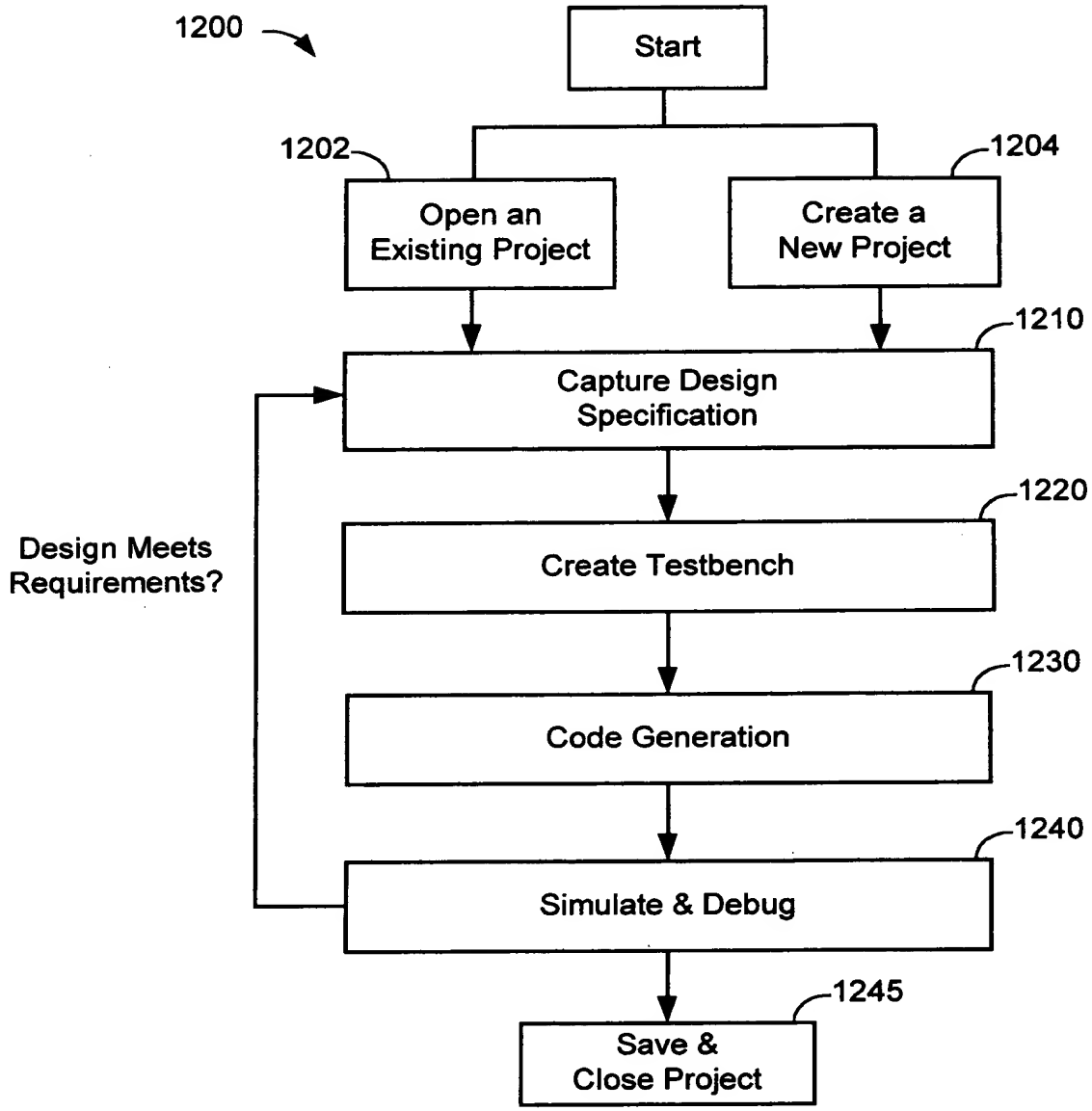
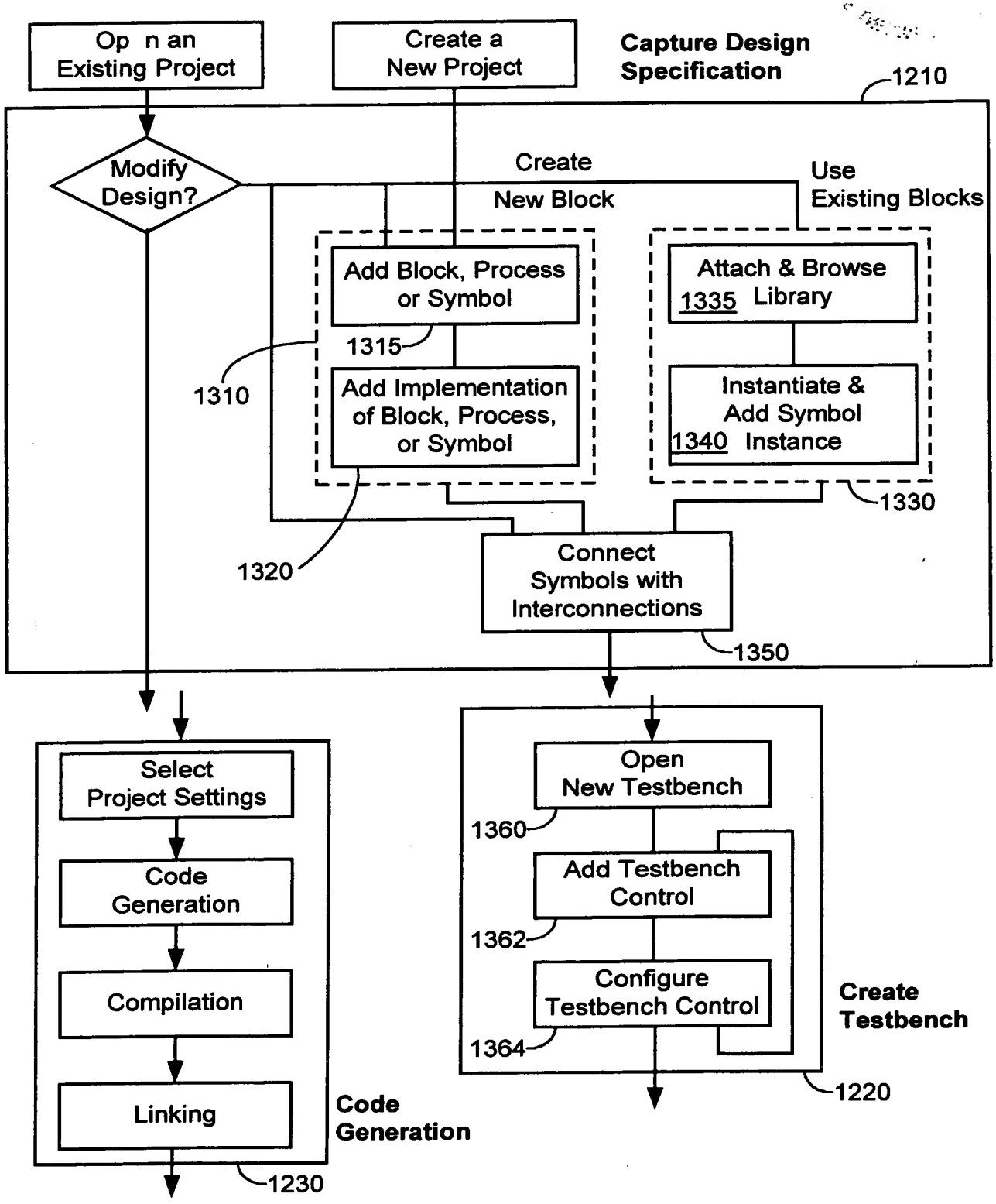

1120
Virtual Testbench/ Human-Machine Interface
API
1104
From C/C++ Based Hardware Modeling Environment
Hardware Debugger
API
1004
Object File for Hardware Specification
Discrete Event Simulation Engine
1002
Hardware Partition
1102
Instruction Set Simulator
1120
1106
Software Partition
Software Debugger
1130

Figure 11


1200
Start
1202
1204
Open an Existing Project
Create a New Project
1210
Capture Design Specification
1220
Create Testbench
Design Meets Requirements?
1230
Code Generation
1240
Simulate & Debug
1245
Save & Close Project

Figur 12


Op n an Existing Project
Create a New Project
Capture Design Specification
1210
Modify Design?
Create New Block
Use Existing Blocks
Add Block, Process or Symbol
1315
1310
Add Implementation of Block, Process, or Symbol
Attach & Browse 1335 Library
Instantiate & Add Symbol 1340 Instance
1330
1320
Connect Symbols with Interconnections
1350
Select Project Settings
Code Generation
Compilation
Linking
Code Generation
1230
Open New Testbench
1360
Add Testbench Control
1362
Configure Testbench Control
1364
Create Testbench
1220

Figur 13

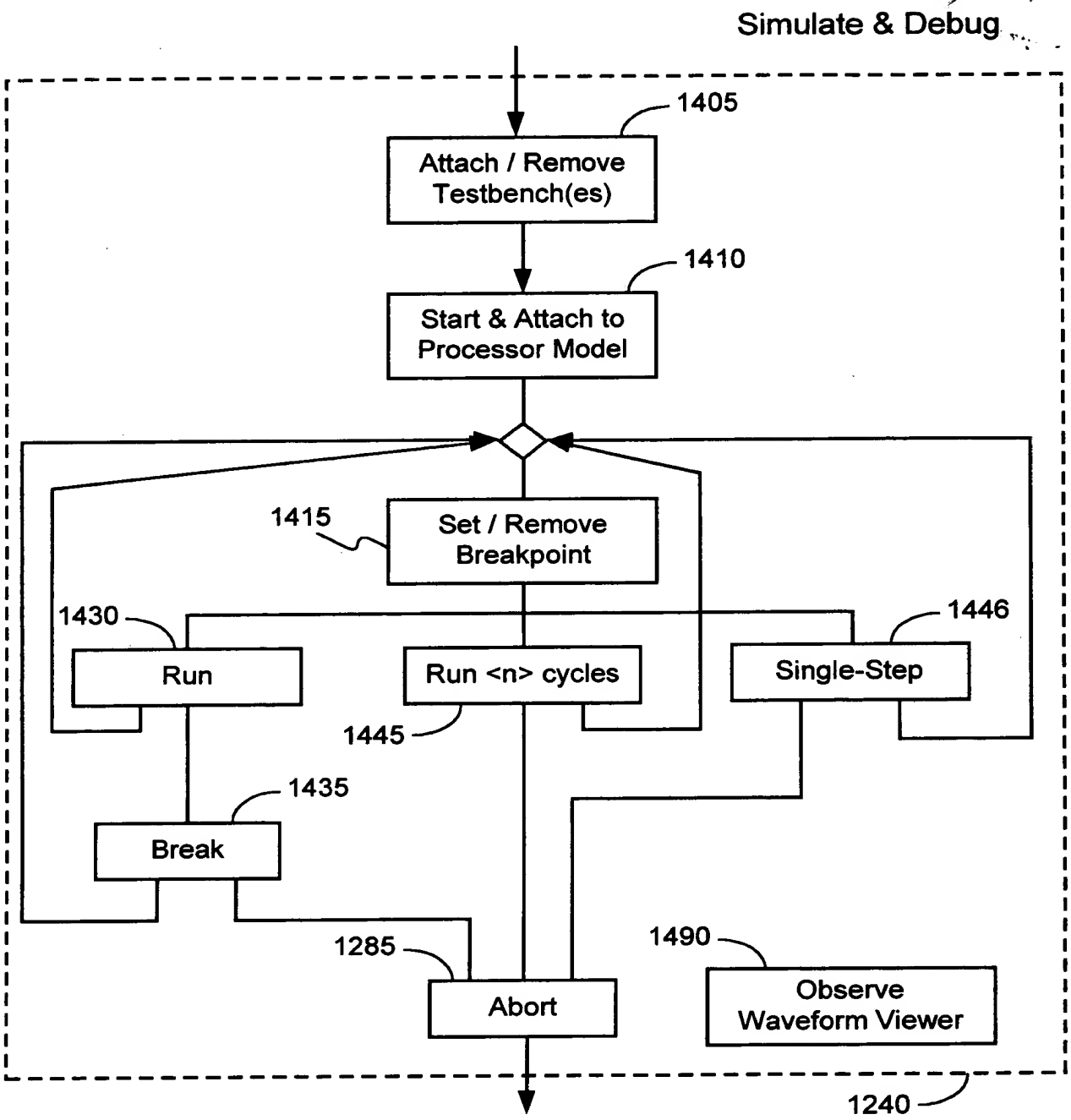

Simulate & Debug
1405
Attach / Remove Testbench(es)
1410
Start & Attach to Processor Model
1415
Set / Remove Breakpoint
1430
Run
Run <n> cycles
1445
1446
Single-Step
1435
Break
1285
Abort
1490
Observe Waveform Viewer
1240

Figure 14

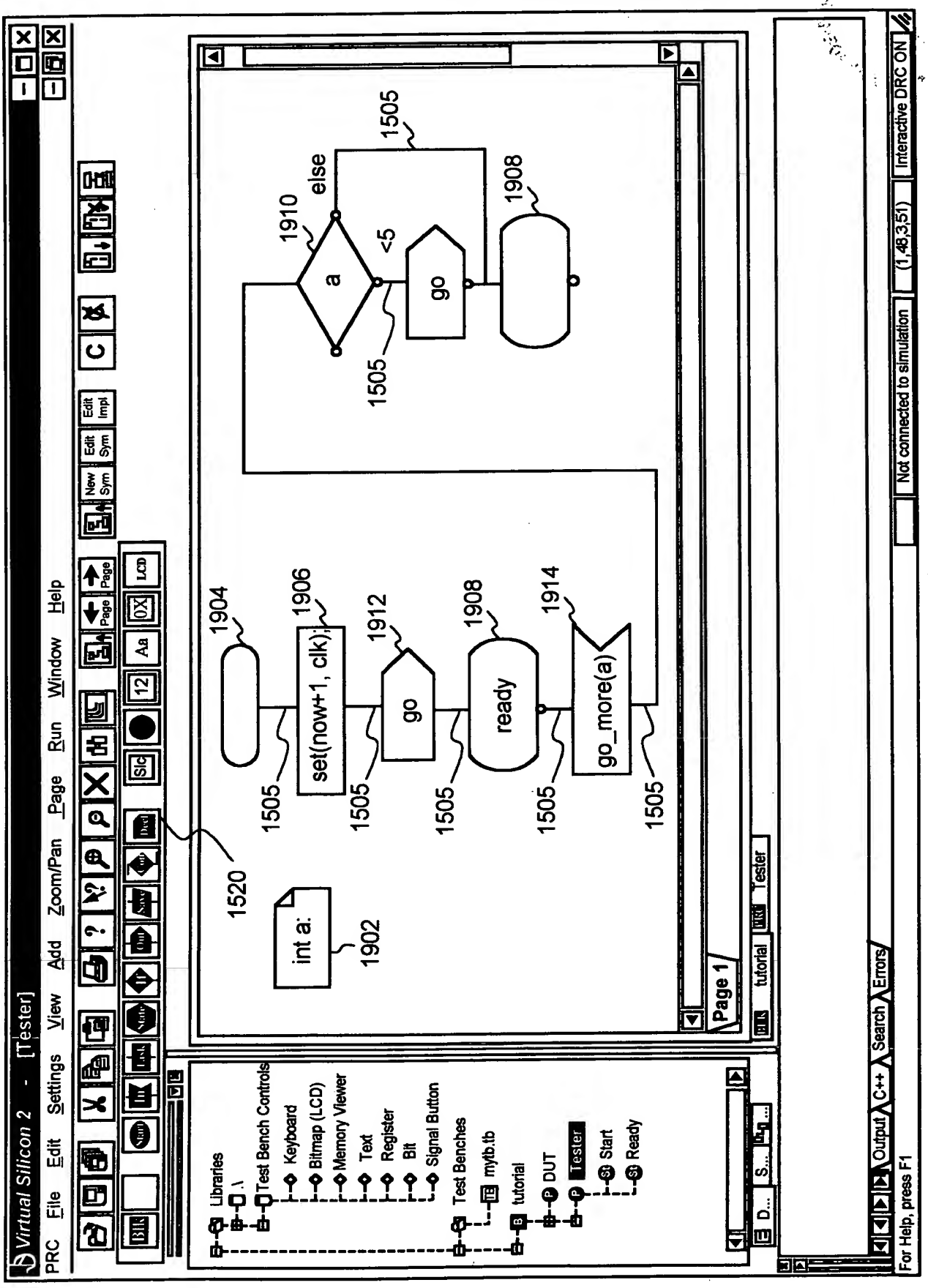

Virtual Silicon 2 - [Tester]
PRC File Edit Settings View Add Zoom/Pan Page Run Window Help
Libraries
Test Bench Controls
Keyboard
Bitmap (LCD)
Memory Viewer
Text
Register
Bit
Signal Button
Test Benches
mytb.tb
tutorial
DUT
Tester
Start
Ready
int a;
1902
1520
1904
1505
set(now+1, clk);
1906
1912
go
1908
ready
1914
go_more(a)
1910
a
else
<5
1908
Page 1
tutorial
Tester
Output
C++
Search
Errors
Not connected to simulation
(1,48,3,51)
Interactive DRC ON
For Help, press F1

Figure 15

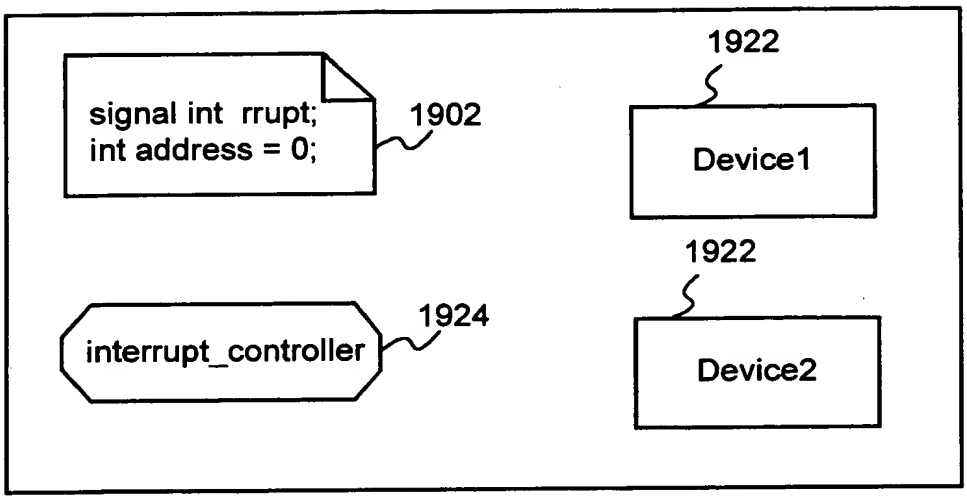


Figure 16

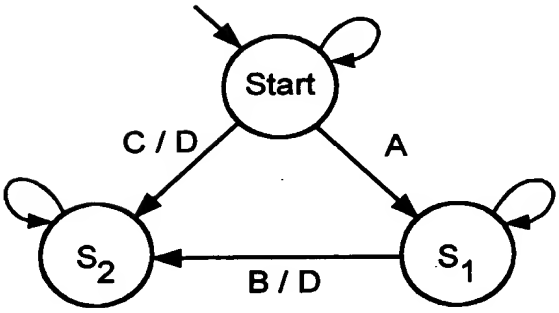


Figure 17(a)

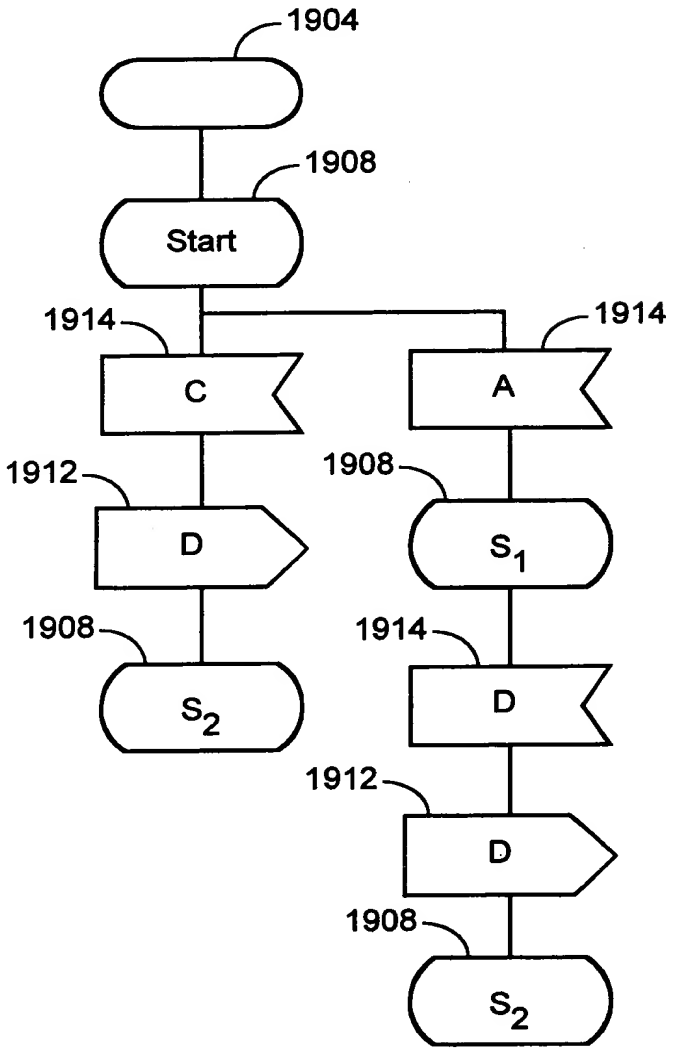
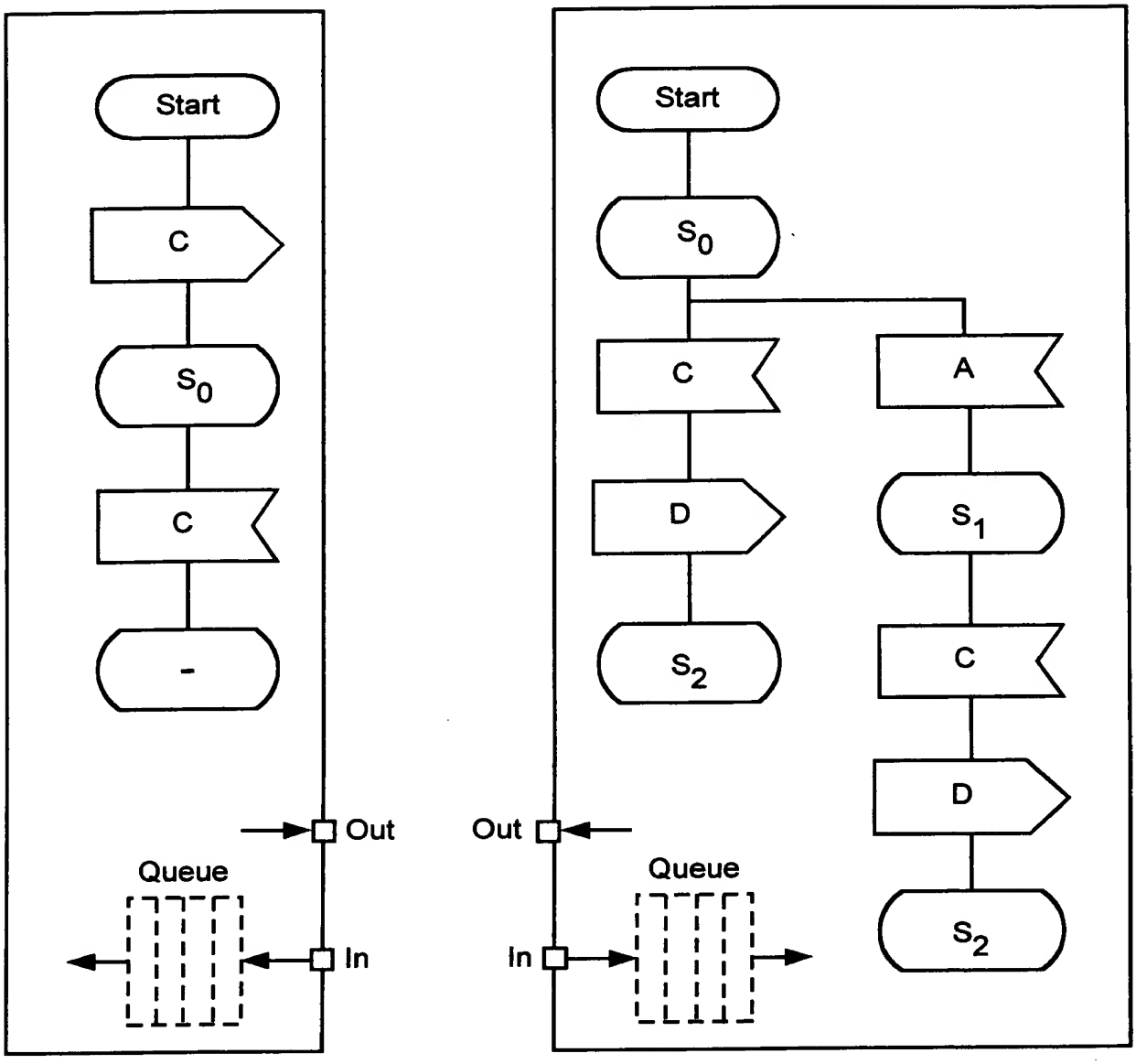


Figure 17(b)



Figur 18

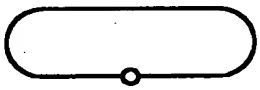
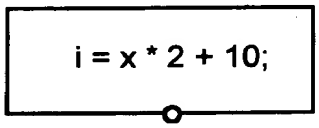
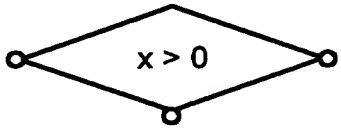
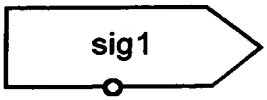
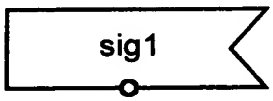
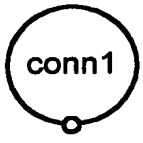
	Name	Graphical Symbol	De cription
1902	Declaration		defines local variables and signals.
1904	Start		Starting point of the Finite State Machine execution at initialization time
1906	Task		Execution block, containing ANSI-C statements to be executed
1908	State		Location where FSM waits in until a triggering signal is received.
1910	Decision		Directs execution flow based on the result of expression evaluation inside the decision construct.
1912	Signal-Out		Sending of a communication signal (with an optional payload)
1914	Signal-In		Receiving of a communication signal (with an optional payload)
1916	Connector		Allows to split designs over multiple pages, and connects the control flow between these diff rent pages.

Figure 19A

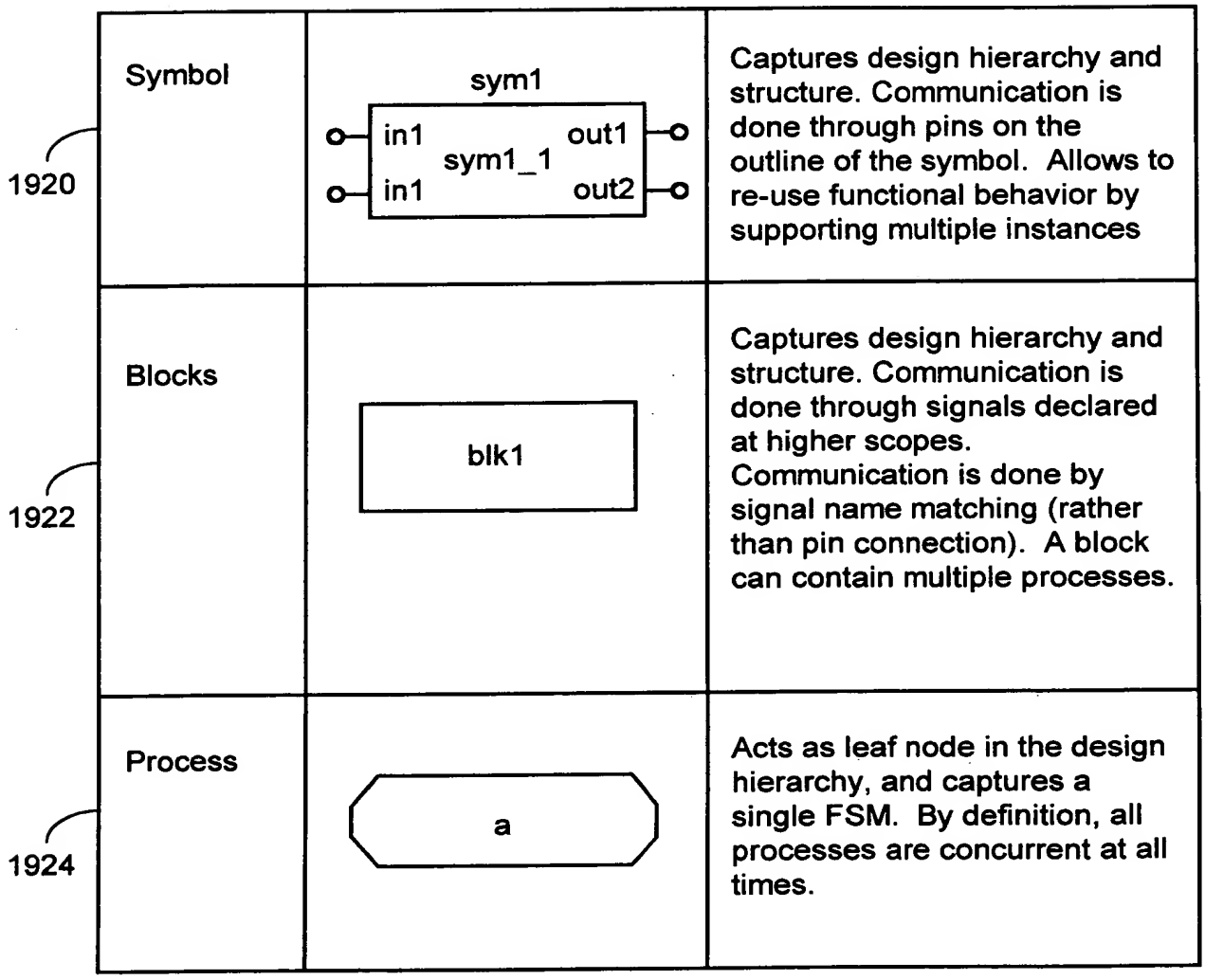
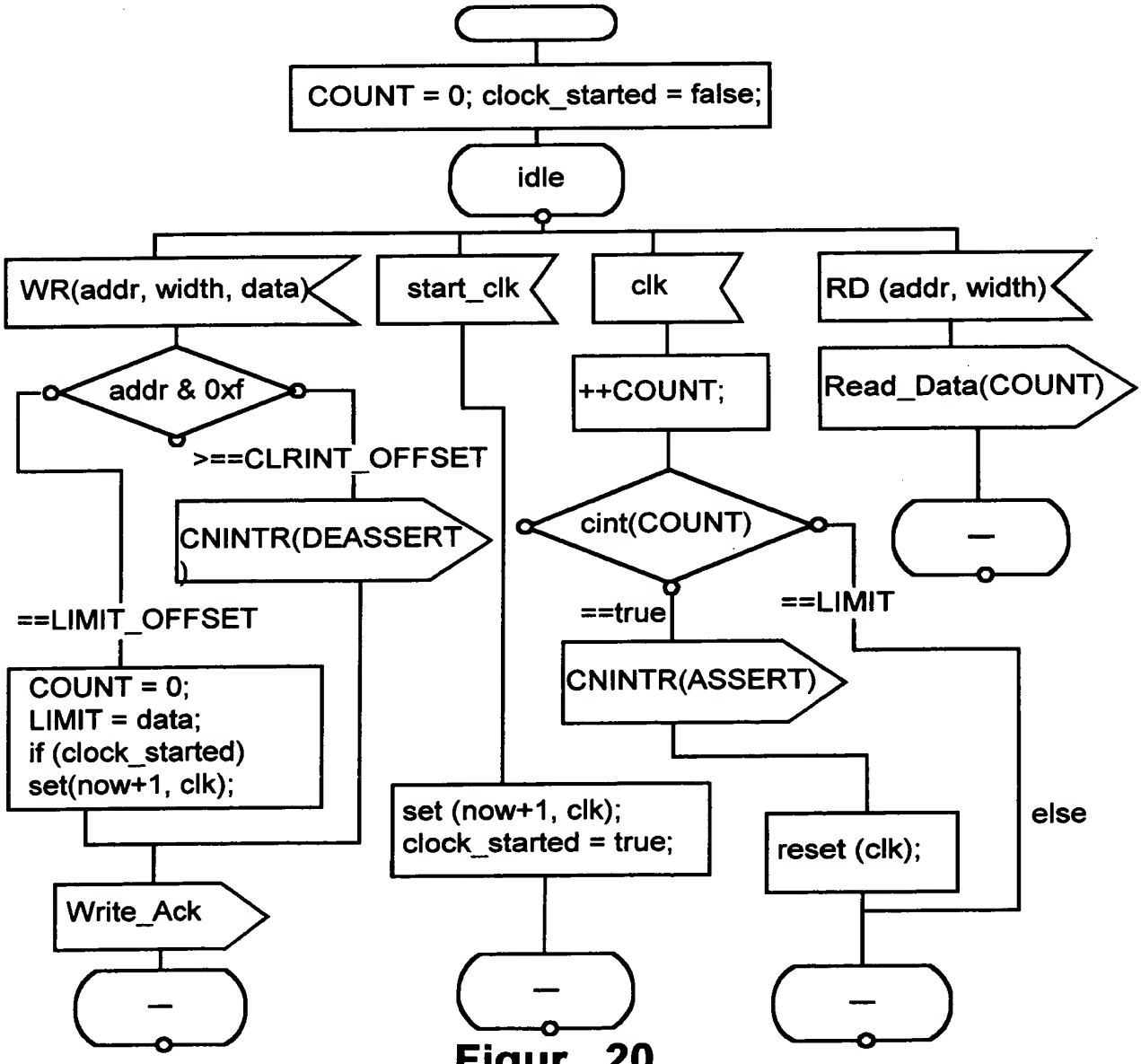

Symbol
sym1
in1
in1
sym1_1
out1
out2
Captures design hierarchy and structure. Communication is done through pins on the outline of the symbol. Allows to re-use functional behavior by supporting multiple instances
1920
Blocks
blk1
Captures design hierarchy and structure. Communication is done through signals declared at higher scopes. Communication is done by signal name matching (rather than pin connection). A block can contain multiple processes.
1922
Process
a
Acts as leaf node in the design hierarchy, and captures a single FSM. By definition, all processes are concurrent at all times.
1924

Figure 19B

```
// External interface
extern_signal WR(unsigned int, unsigned int,
unsigned int);
extern_signal RD(unsigned int, unsigned int);
extern_signal Write_Ack;
extern_signal Read_Data(unsigned int);
extern_signal CNTINTR(unsigned int);
// Local variables
signal start_clk;
clock clk;
bool clock_started;
unsigned int LIMIT; //write register
VS_int COUNT;
//temp vars
unsigned int data, width, addr;
```



Figur 20

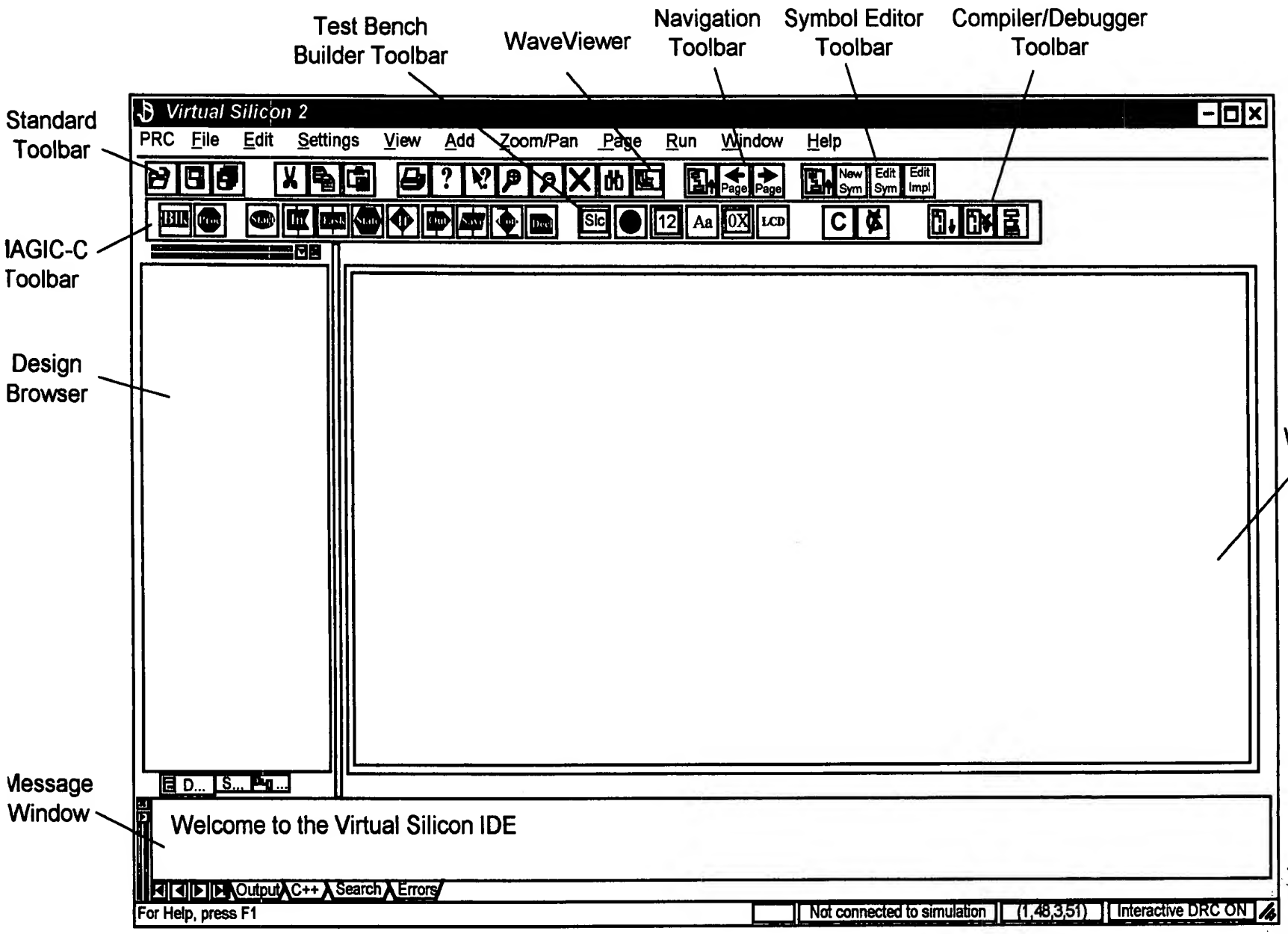


Figure 21

Application No. 09/872,435
Title: METHOD AND SYSTEM FOR VIRTUAL PROTOTYPING
Inventor(s): Stephen L. Bade et al.
Atty. Docket No.: 22178-05012
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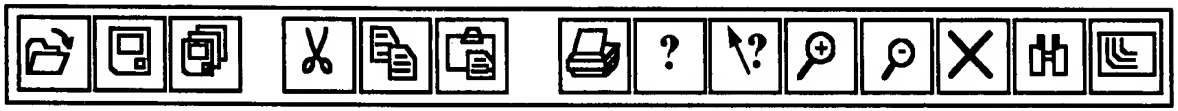
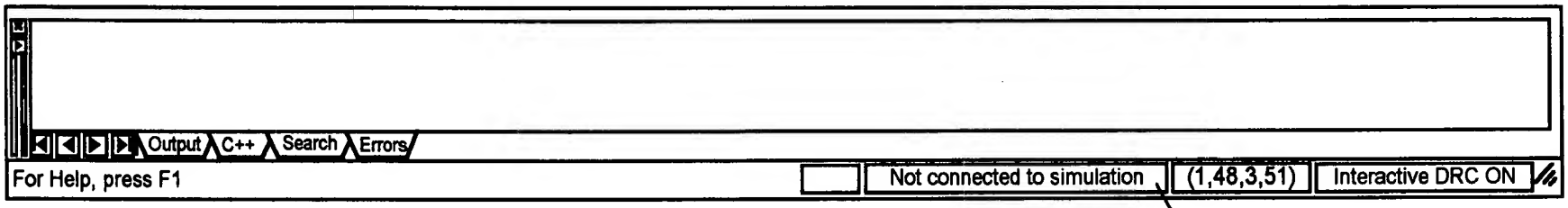


Standard Toolbar

Figure 22



Message Window, Showing Different Message Tabs, and the Status Bar

Status Bar

Figure 23

Application No. 09/872,435
Title: METHOD AND SYSTEM FOR VIRTUAL PROTOTYPING
Inventor(s): Stephen L. Bade et al.
Atty. Docket No.: 22178-05012
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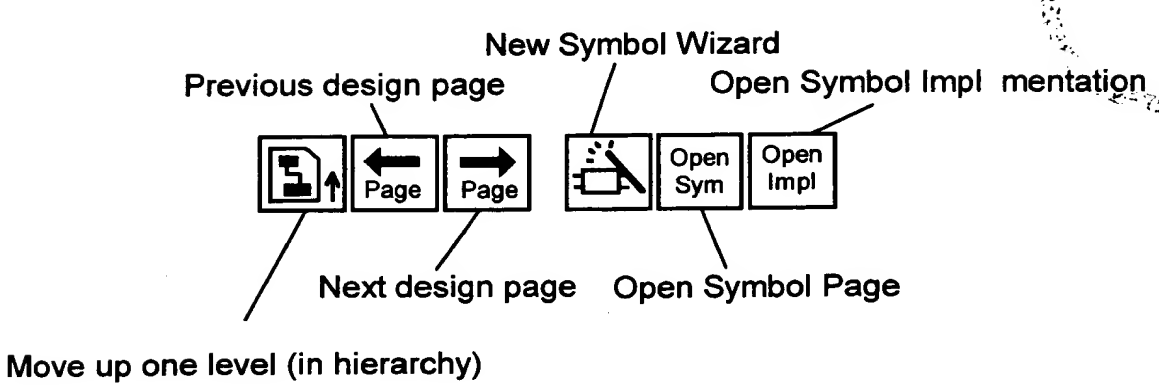


Figure 23

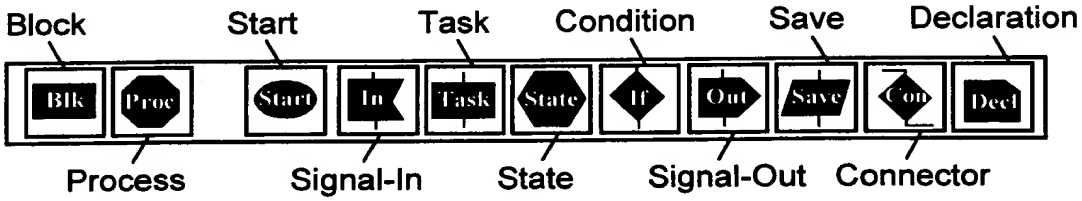


Figure 24

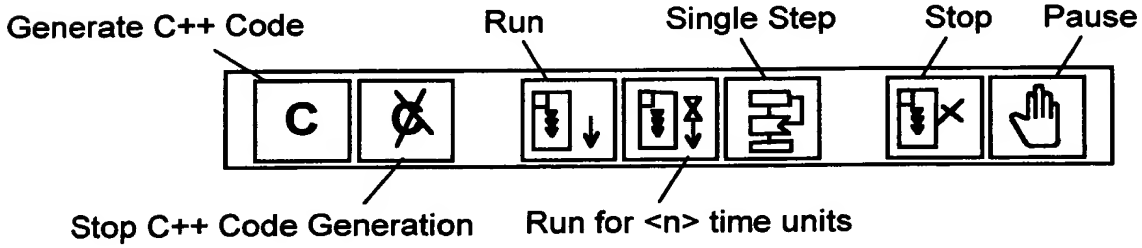


Figure 25

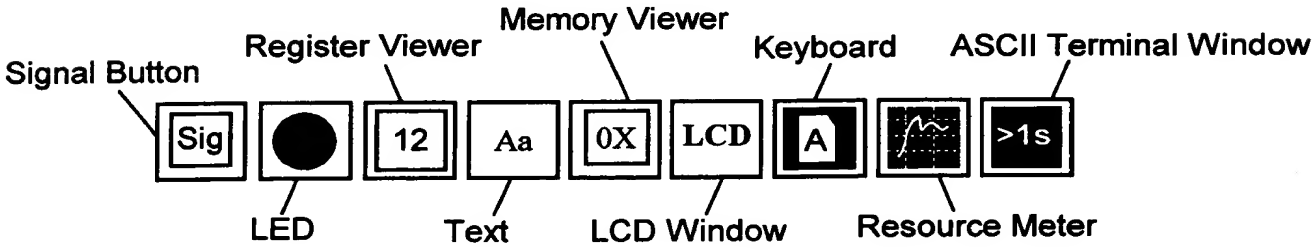


Figure 26

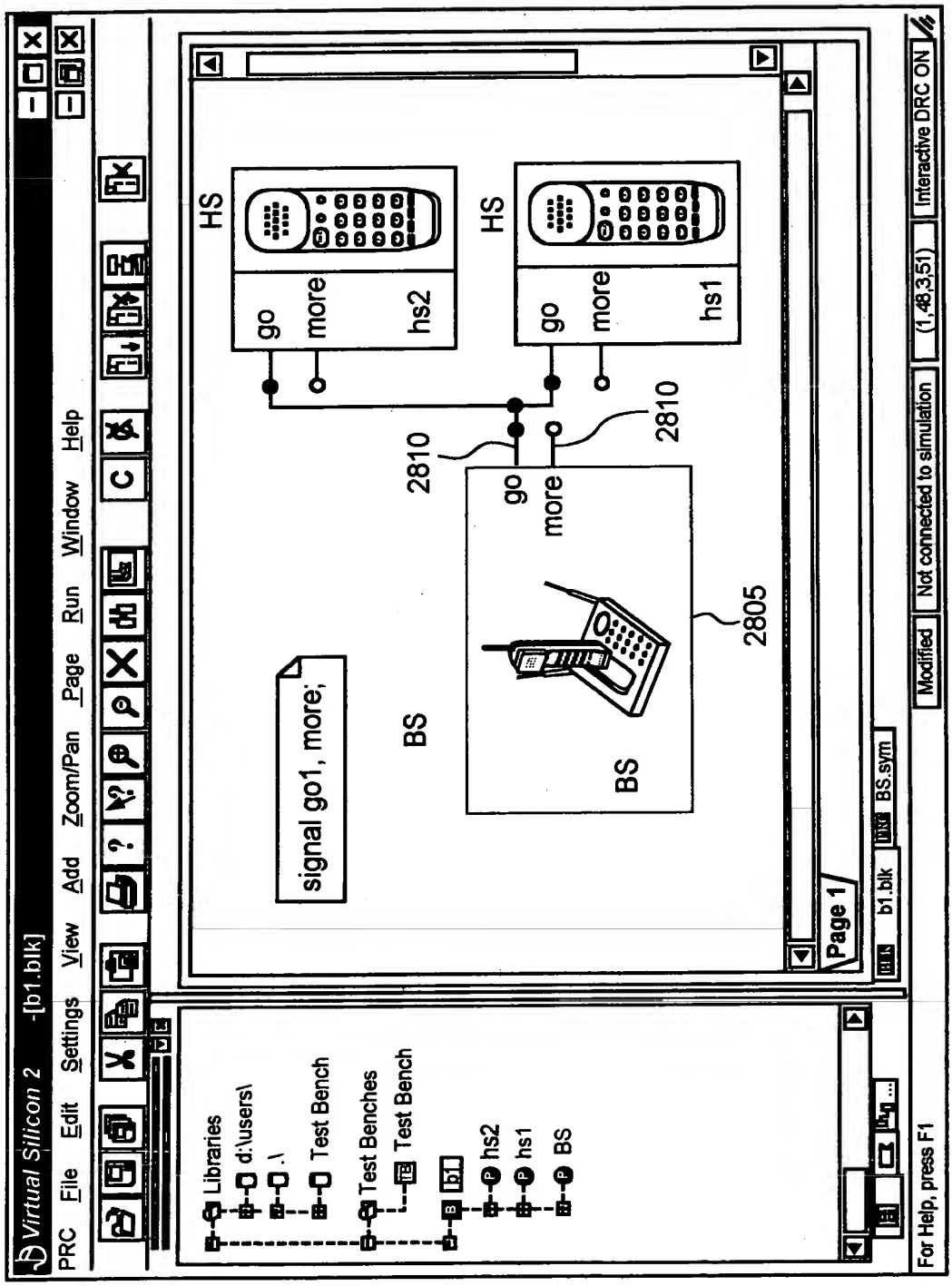

Virtual Silicon 2 -[b1.blk]
PRC File Edit Settings View Add Zoom/Pan Page Run Window Help
Libraries
d:\users\
.\
Test Bench
Test Benches
Test Bench
b1
hs2
hs1
BS
HS
go
more
hs2
HS
go
more
hs1
2810
2810
go
more
BS
2805
signal go1, more;
Page 1
b1.blk
BS.sym
Modified
Not connected to simulation
(1,48,3,51)
Interactive DRC ON
For Help, press F1

Figure 28

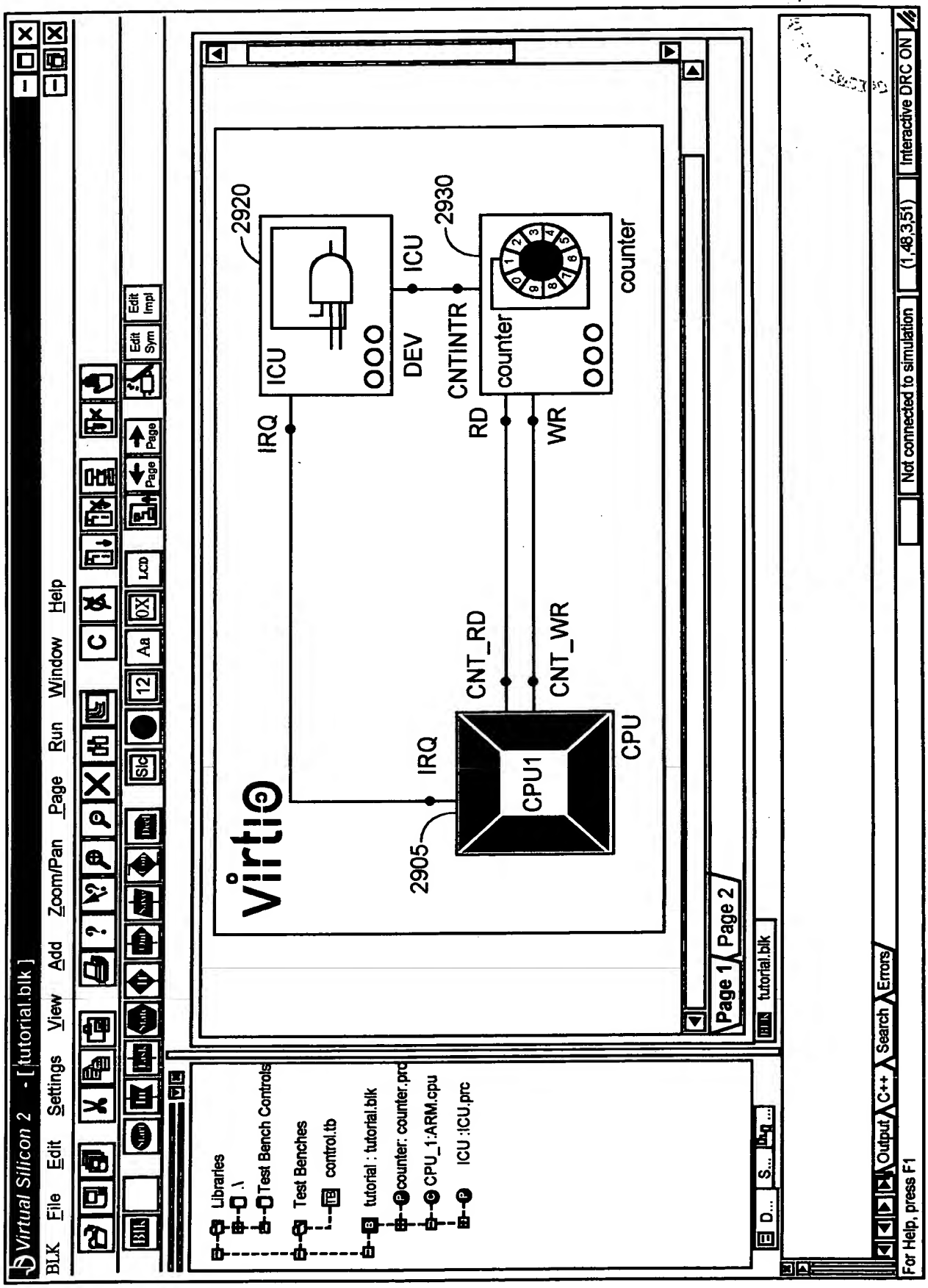

Virtual Silicon 2 - [tutorial.blk]
File Edit Settings View Add Zoom/Pan Page Run Window Help
Libraries
Test Bench Controls
Test Benches
control.tb
tutorial : tutorial.blk
counter: counter.prc
CPU_1:ARM.cpu
ICU :ICU.prc
2920
ICU
IRQ
DEV
ICU
2930
CNTINTR
counter
RD
WR
CNT_RD
CNT_WR
IRQ
CPU1
CPU
2905
Page 1
Page 2
tutorial.blk
Output
C++
Search
Errors
Not connected to simulation
(1,48,3,51)
Interactive DRC ON
For Help, press F1

Figure 29

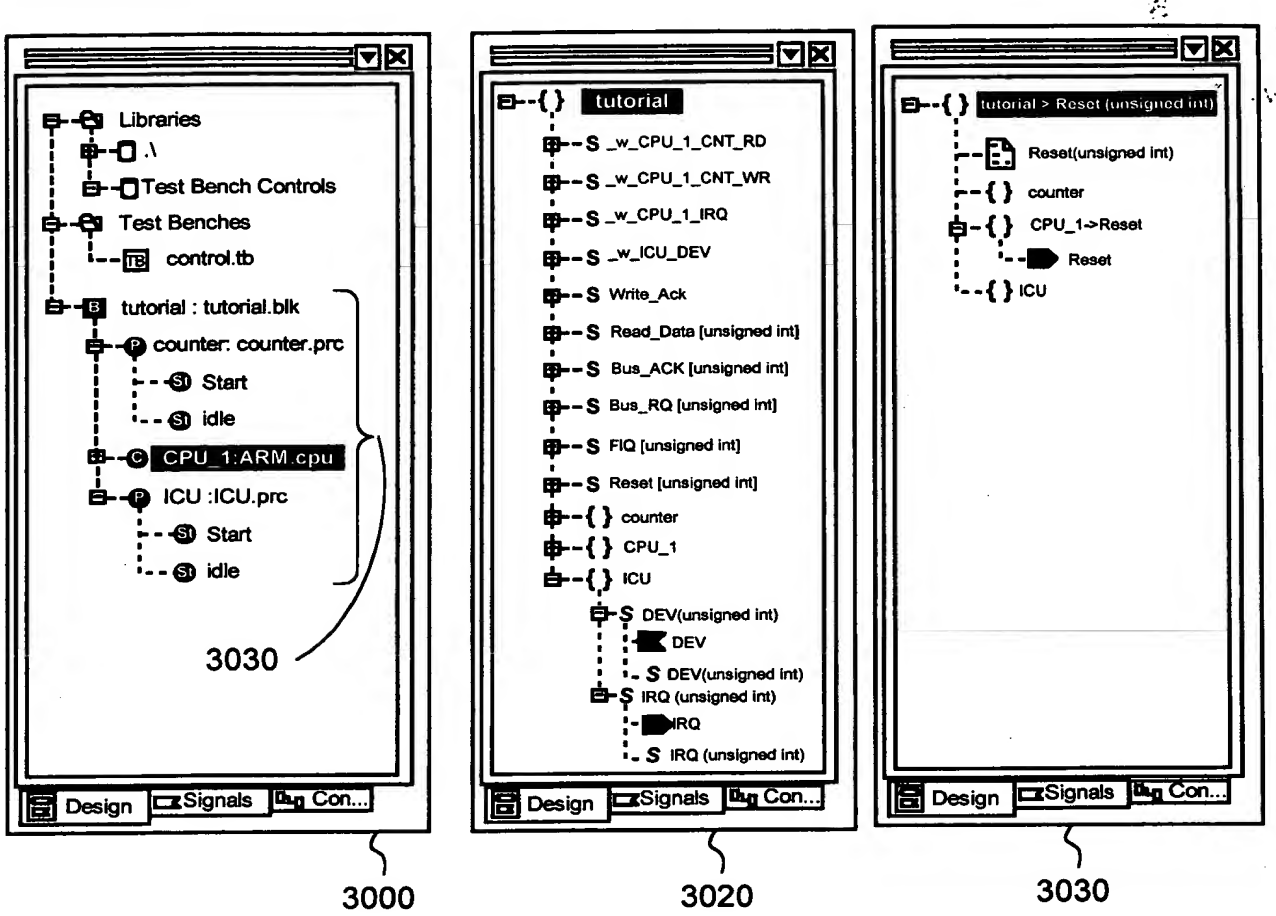
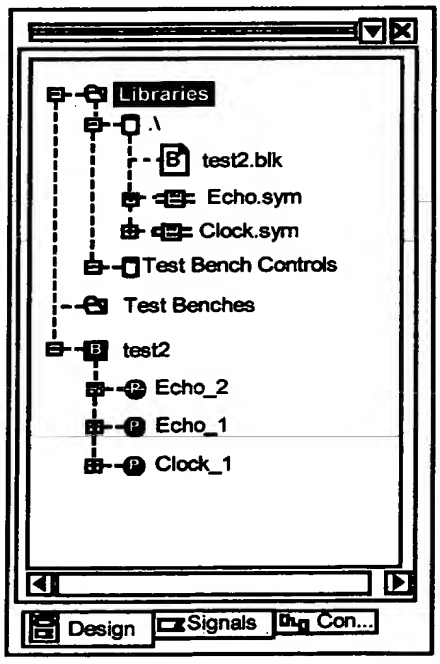


Figure 30



Figur 31

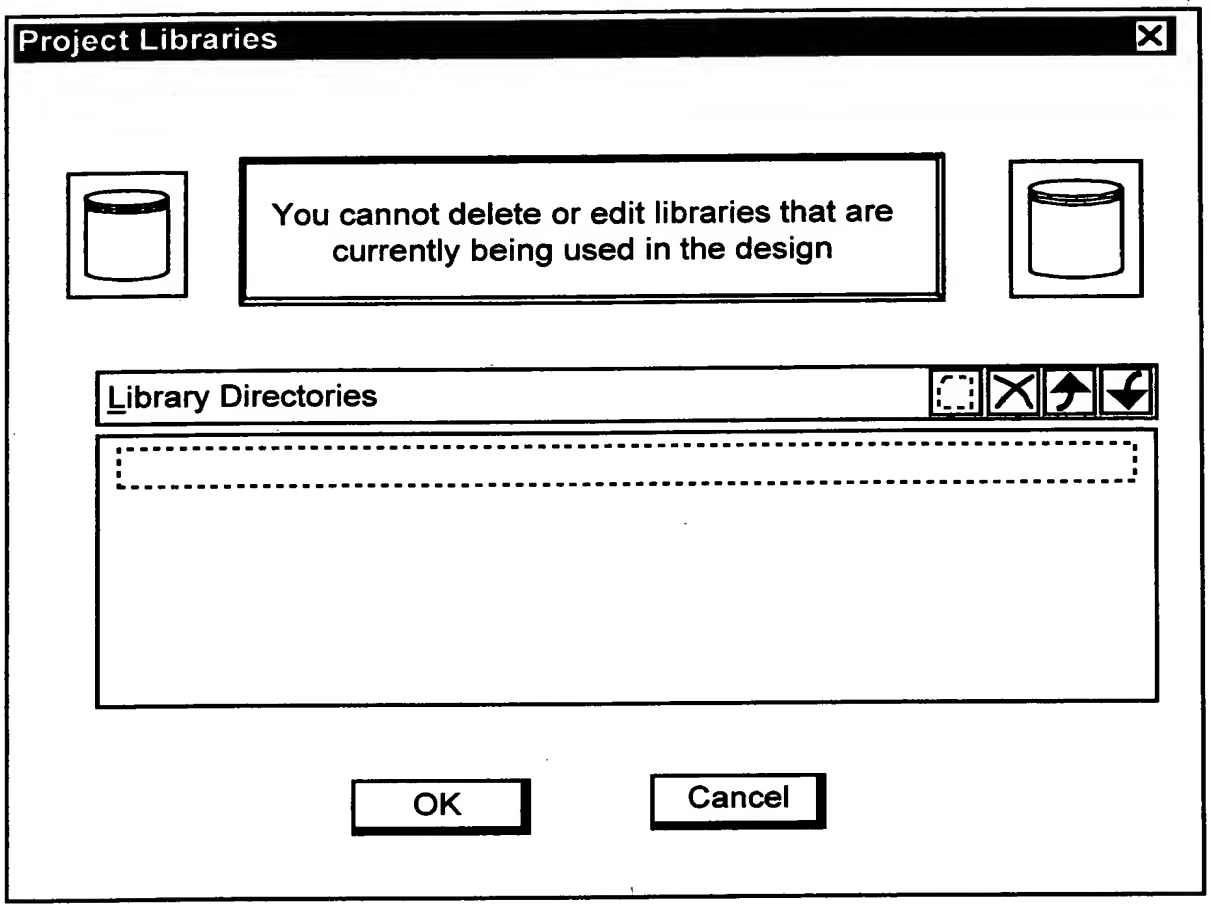

Project Libraries
You cannot delete or edit libraries that are currently being used in the design
Library Directories
OK
Cancel

Figure 32

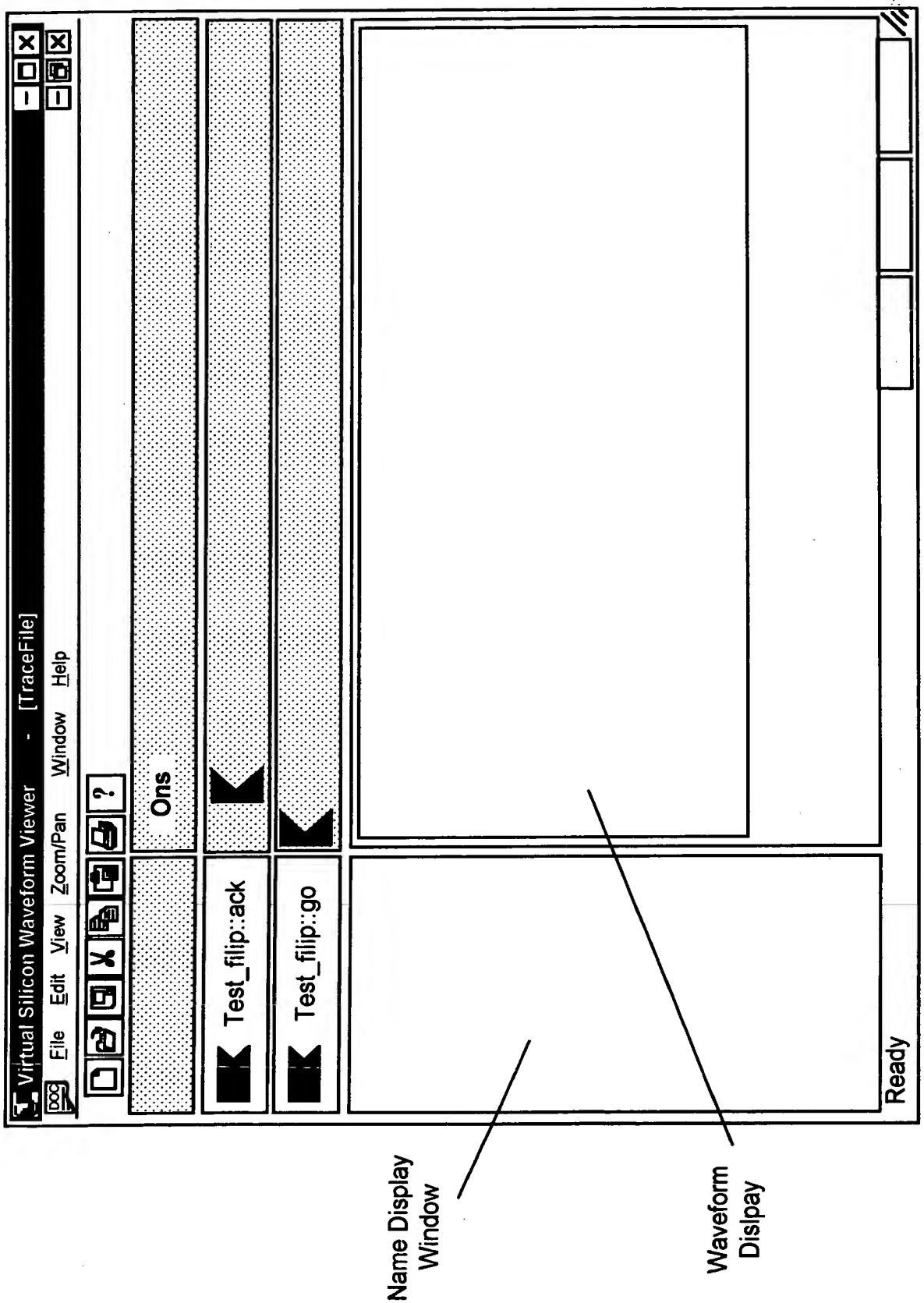

Virtual Silicon Waveform Viewer - [TraceFile]
File Edit View Zoom/Pan Window Help
Ons
Test_filip::ack
Test_filip::go
Ready
Name Display Window
Waveform Dislpay

Figure 33A

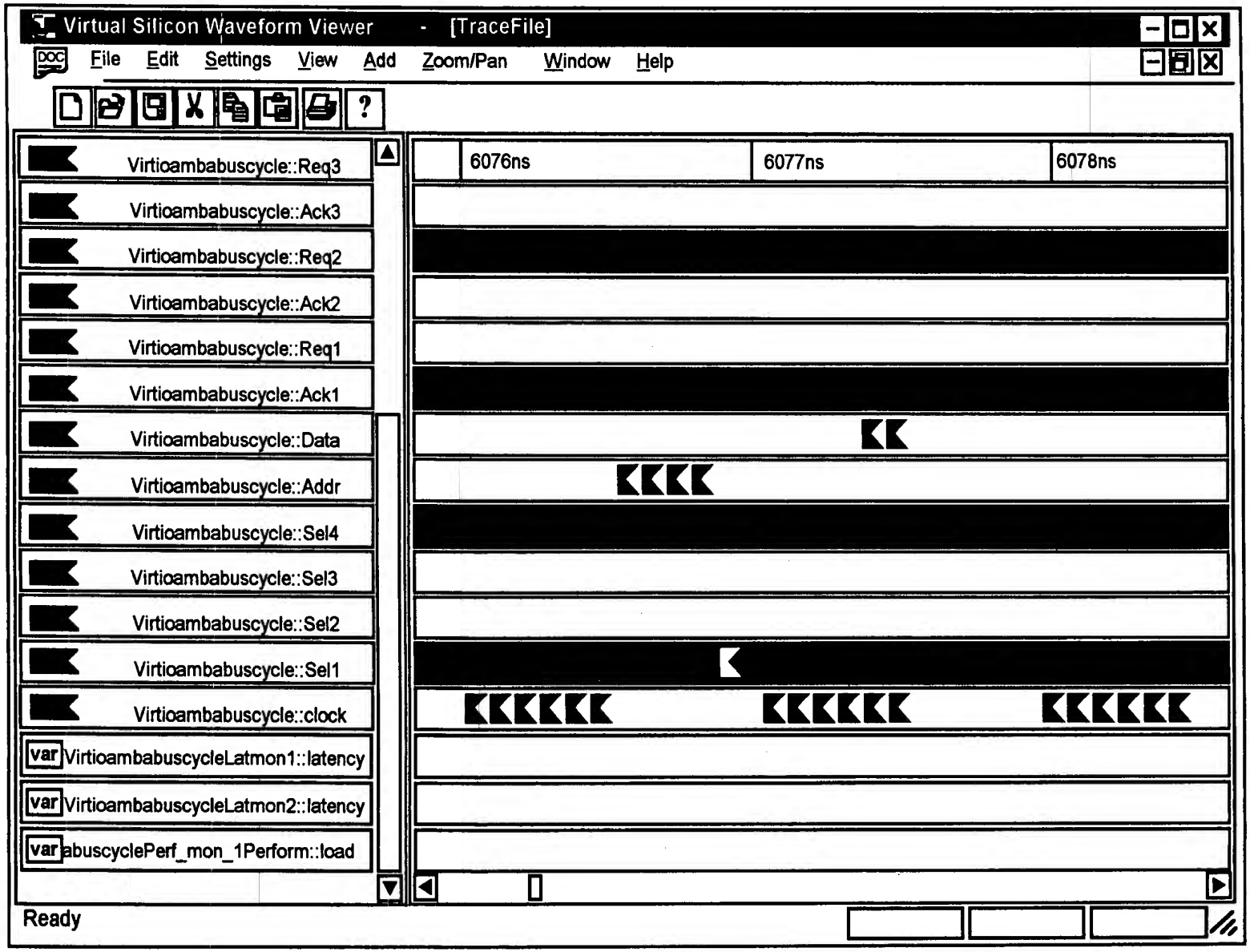


Figure 33B

Application No. 09/872,435
Title: METHOD AND SYSTEM FOR VIRTUAL PROTOTYPING
Inventor(s): Stephen L. Bade et al.
Atty. Docket No.: 22178-05012
Sheet 30 of 65

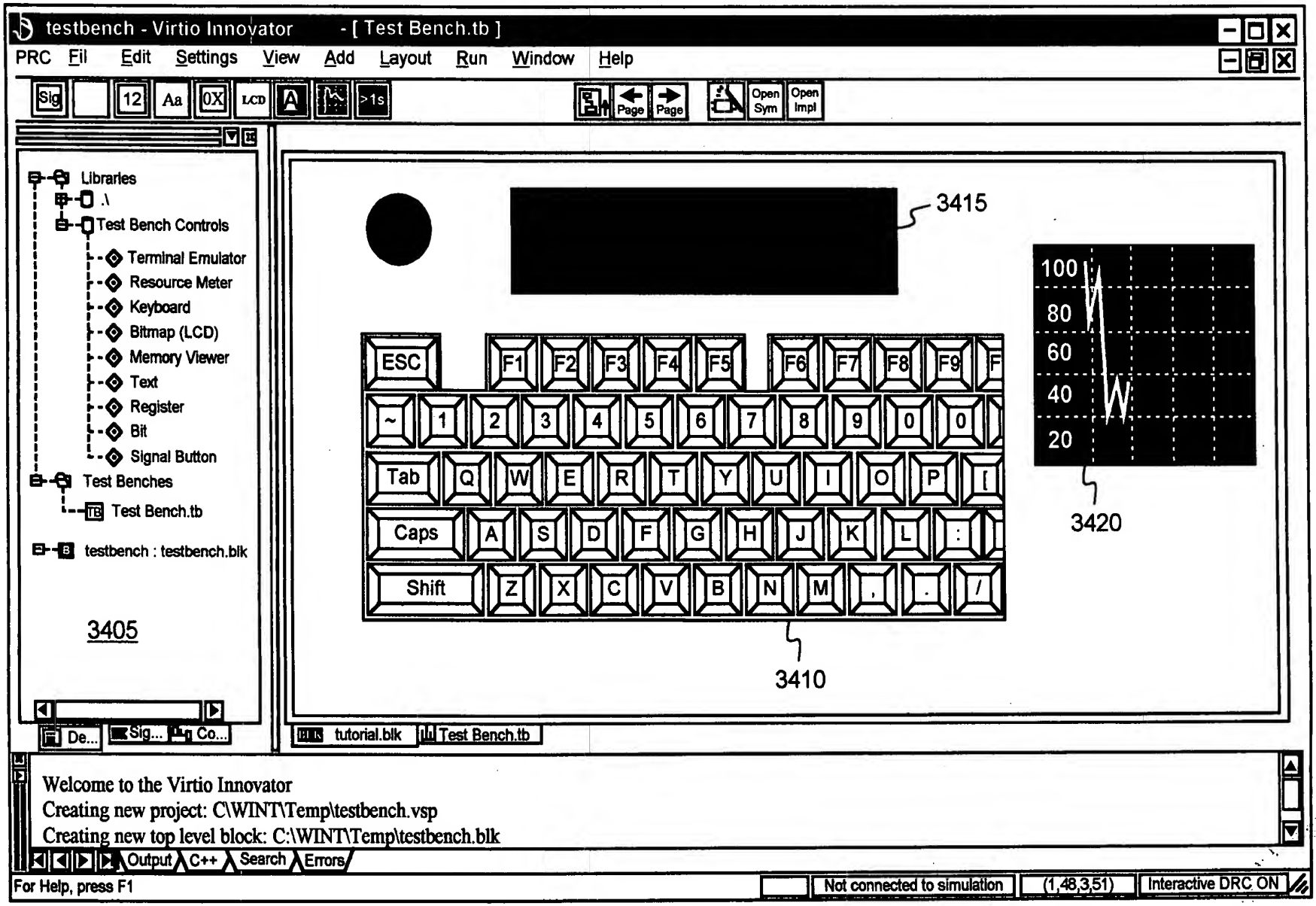


Figure 34A

Application No. 09/872,435
Title: METHOD AND SYSTEM FOR VIRTUAL PROTOTYPING
Inventor(s): Stephen L. Bade et al.
Atty. Docket No.: 22178-05012
Sheet 31 of 65

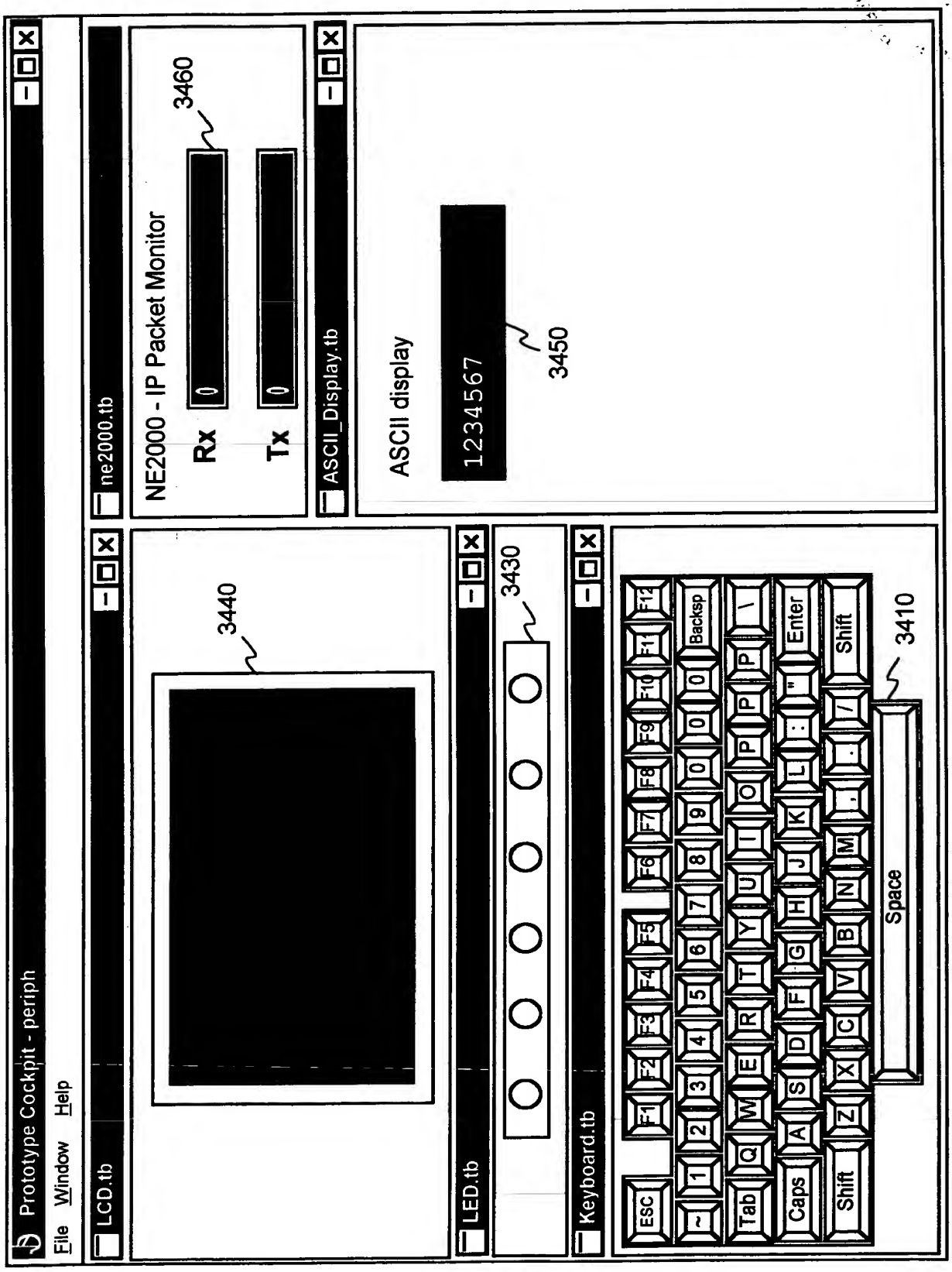

Prototype Cockpit - periph
File Window Help
LCD.tb
3440
LED.tb
3430
ne2000.tb
NE2000 - IP Packet Monitor
3460
Rx
Tx
0
0
ASCII_Display.tb
ASCII display
1234567
3450
Keyboard.tb
3410

Figure 34B

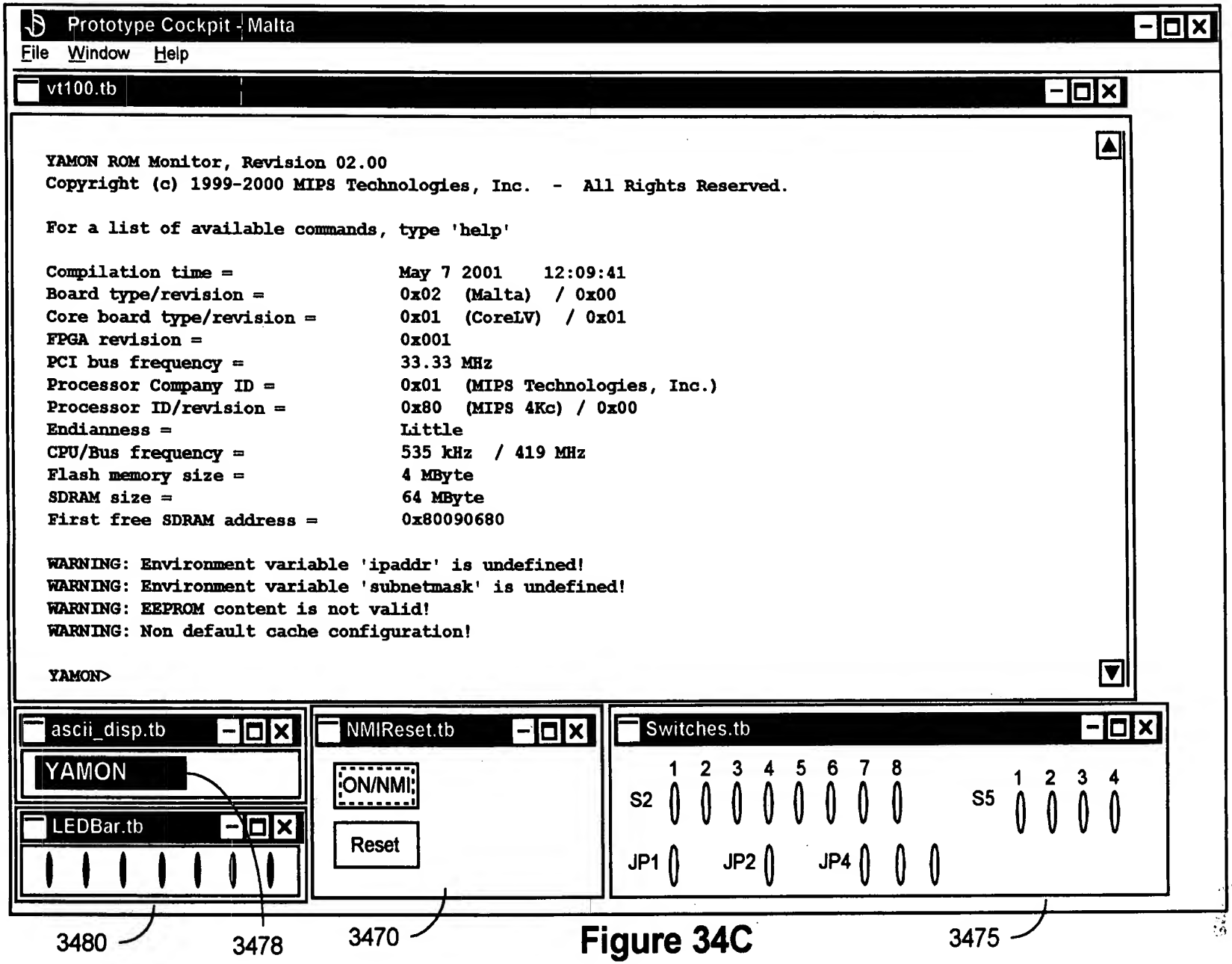


Figure 34C

Application No. 09/872,435
Title: METHOD AND SYSTEM FOR VIRTUAL PROTOTYPING
Inventor(s): Stephen L. Bade et al.
Atty. Docket No.: 22178-05012
Sheet 33 of 65

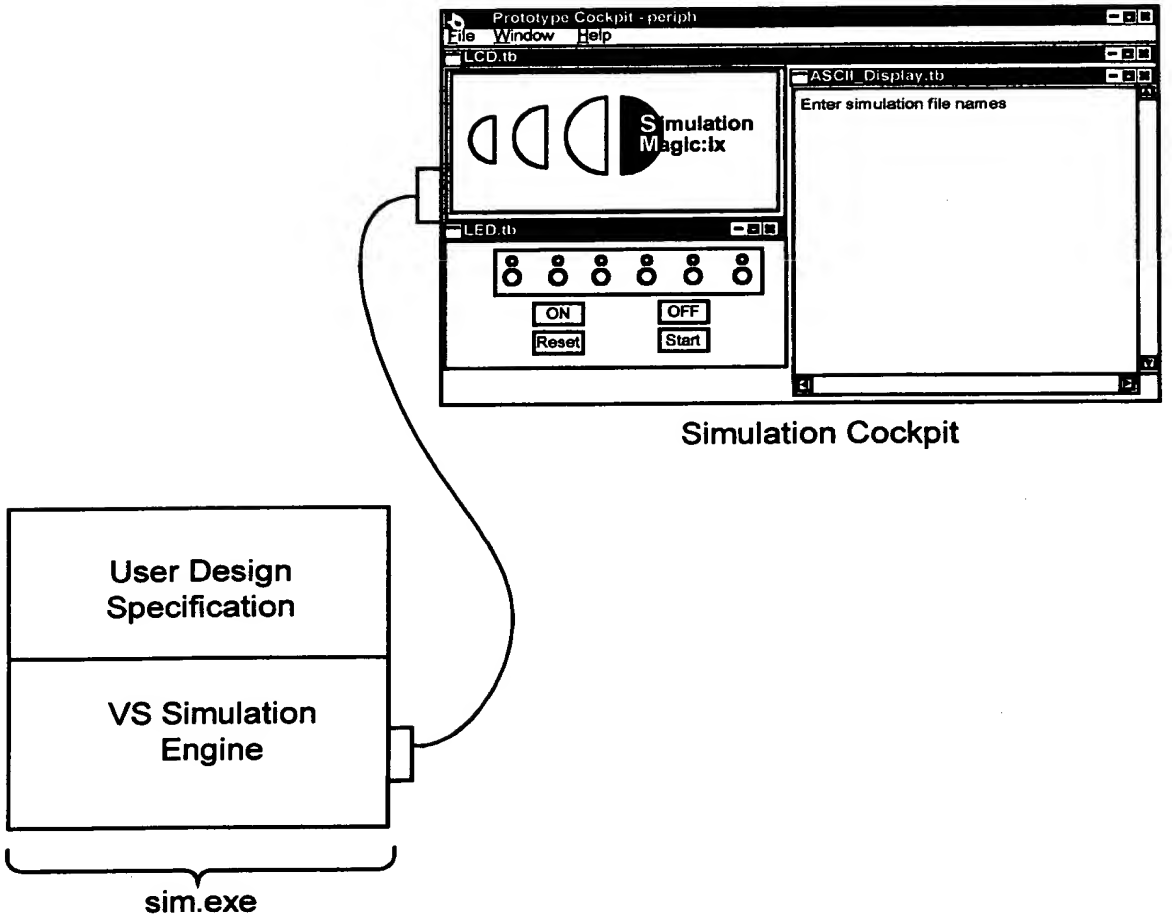

Prototype Cockpit - periph
File Window Help
LCD.tb
Simulation Magic:lx
LED.tb
ON
Reset
OFF
Start
ASCII_Display.tb
Enter simulation file names
Simulation Cockpit
User Design Specification
VS Simulation Engine
sim.exe

Figure 35

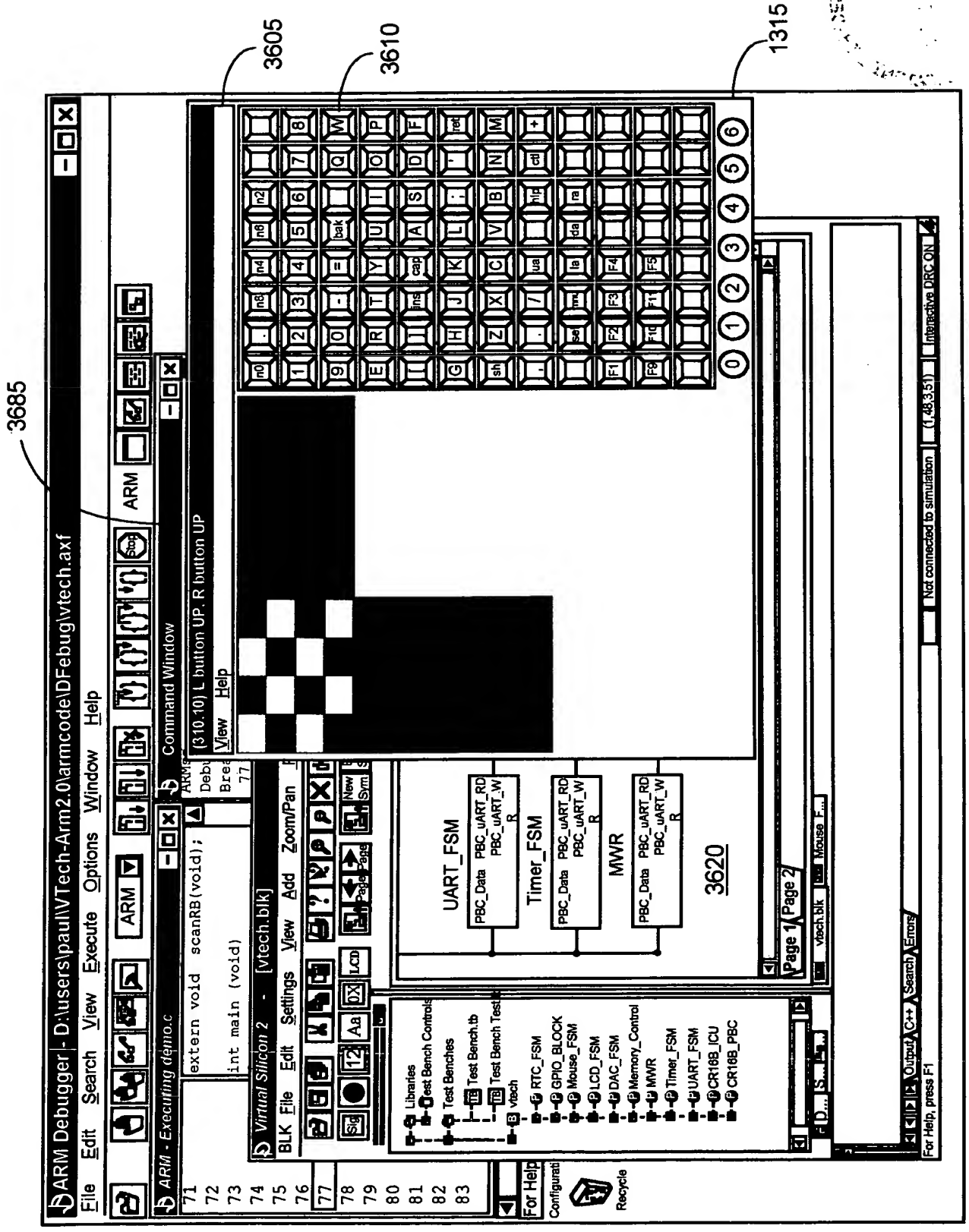

3685
3605
3610
1315
3620
ARM Debugger - D:\users\paul\VTech-Arm2.0\armcode\DFebug\vtech.axf
File Edit Search View Execute Options Window Help
ARM - Executing demo.c
Command Window
[310,10] L button UP. R button UP
View Help
Virtual Silicon 2 - [vtech.blk]
BLK File Edit Settings View Add Zoom/Pan
UART_FSM
Timer_FSM
MWR
PBC_Data
PBC_uART_RD
PBC_uART_W
Page 1
Page 2
Not connected to simulation
Interactive DRC ON
For Help, press F1

Figure 36A

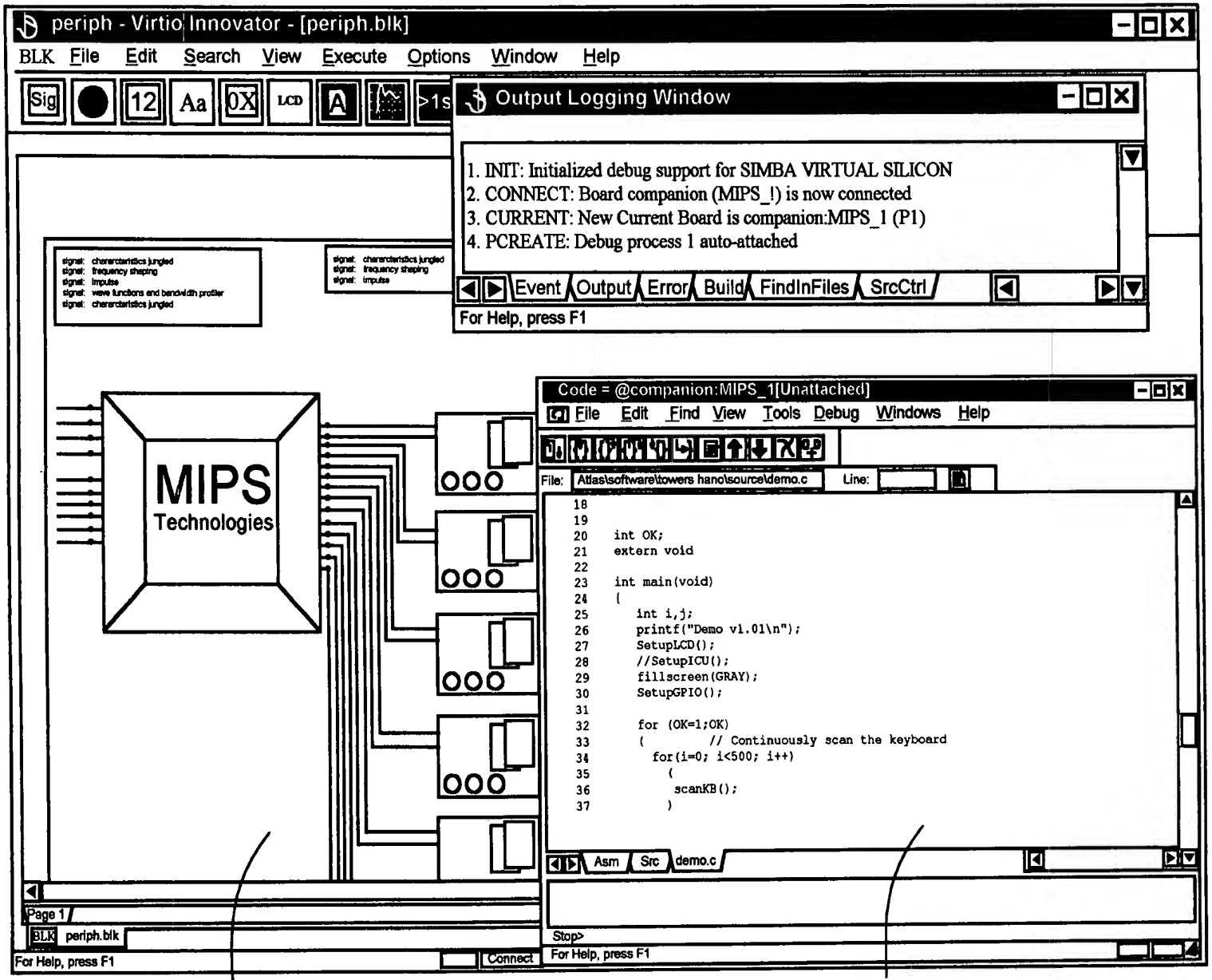


Figure 36B

Application No. 09/872,435
Title: METHOD AND SYSTEM FOR VIRTUAL PROTOTYPING
Inventor(s): Stephen L. Bade et al.
Atty. Docket No.: 22178-05012
Sheet 36 of 65

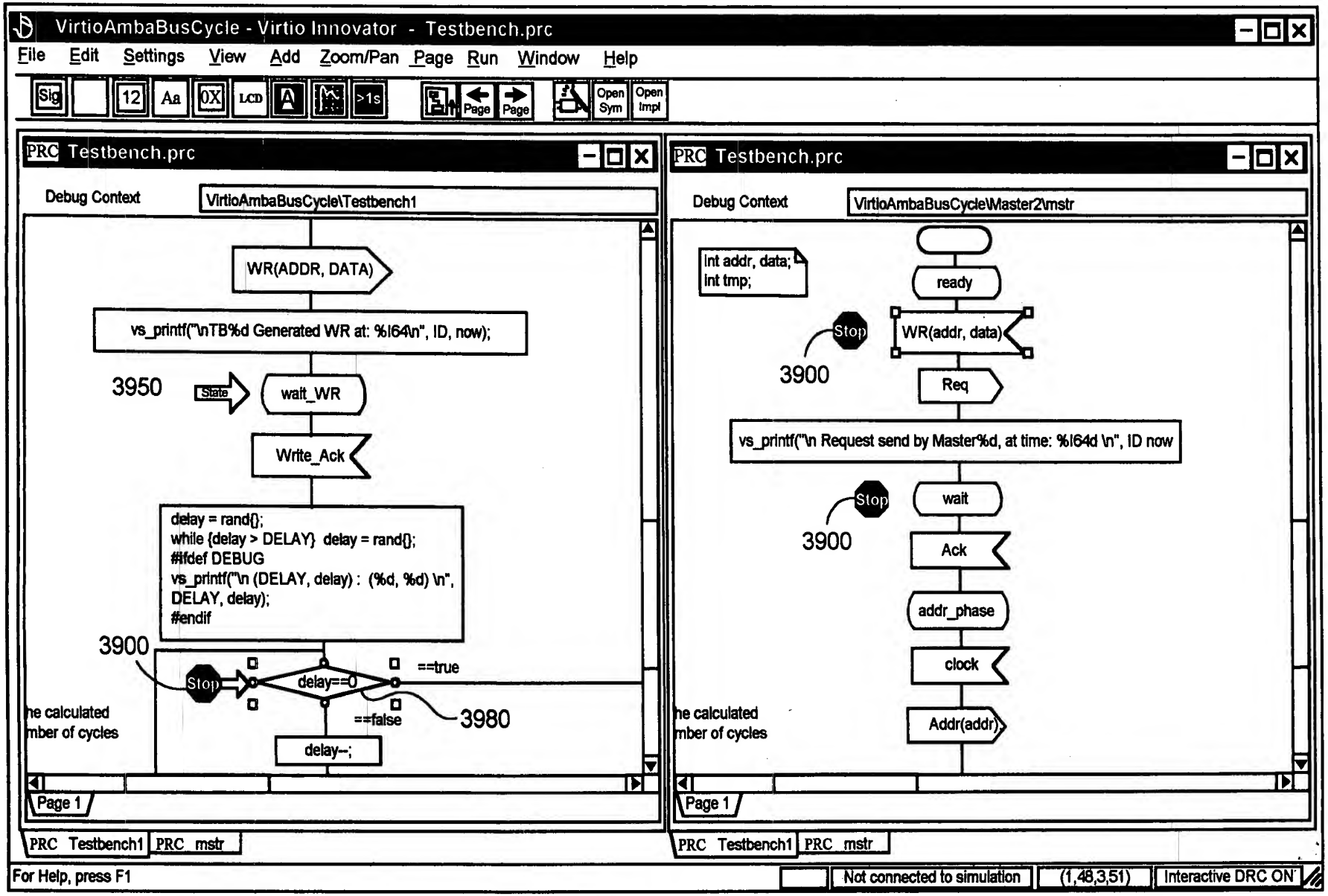


Figure 36C

Application No. 09/872,435
Title: METHOD AND SYSTEM FOR VIRTUAL PROTOTYPING
Inventor(s): Stephen L. Bade et al.
Atty. Docket No.: 22178-05012
Sheet 37 of 65

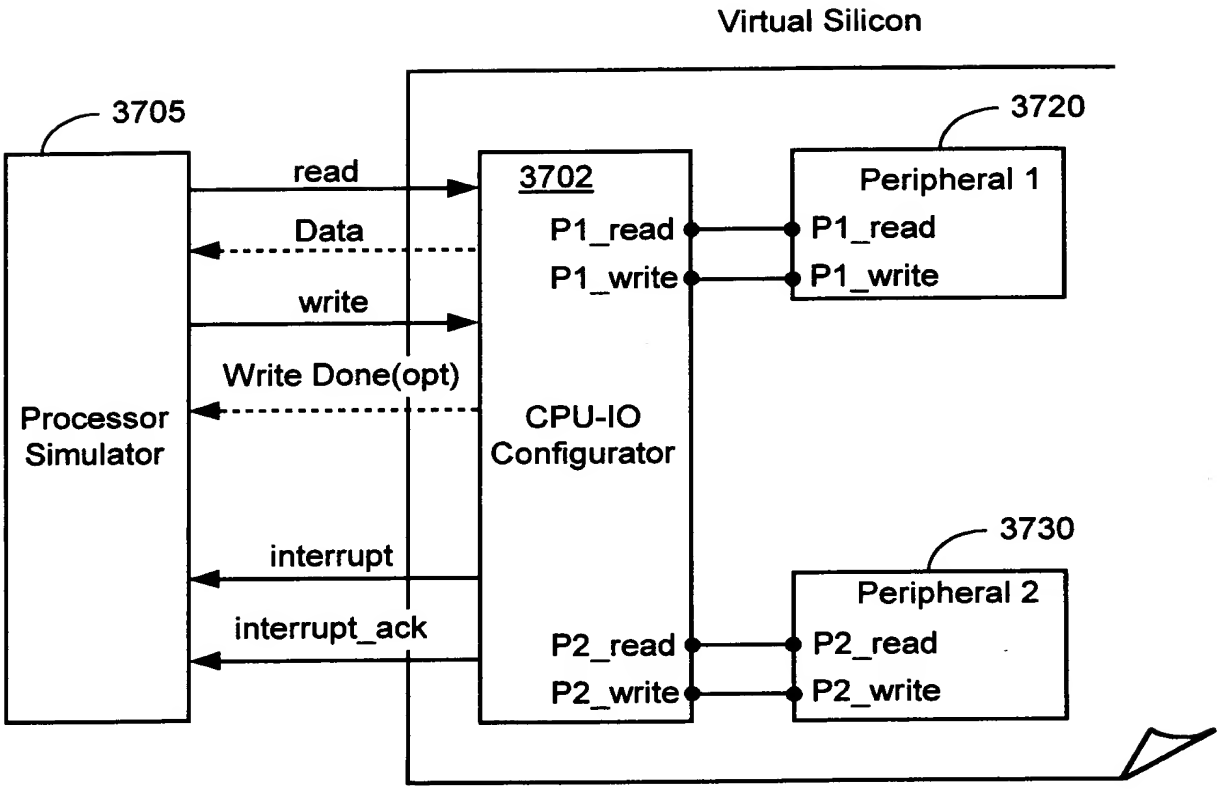

Virtual Silicon
3705
3720
read
3702
Peripheral 1
Data
P1_read
P1_read
P1_write
P1_write
write
Write Done(opt)
Processor Simulator
CPU-IO Configurator
3730
interrupt
Peripheral 2
interrupt_ack
P2_read
P2_read
P2_write
P2_write

Figure 37

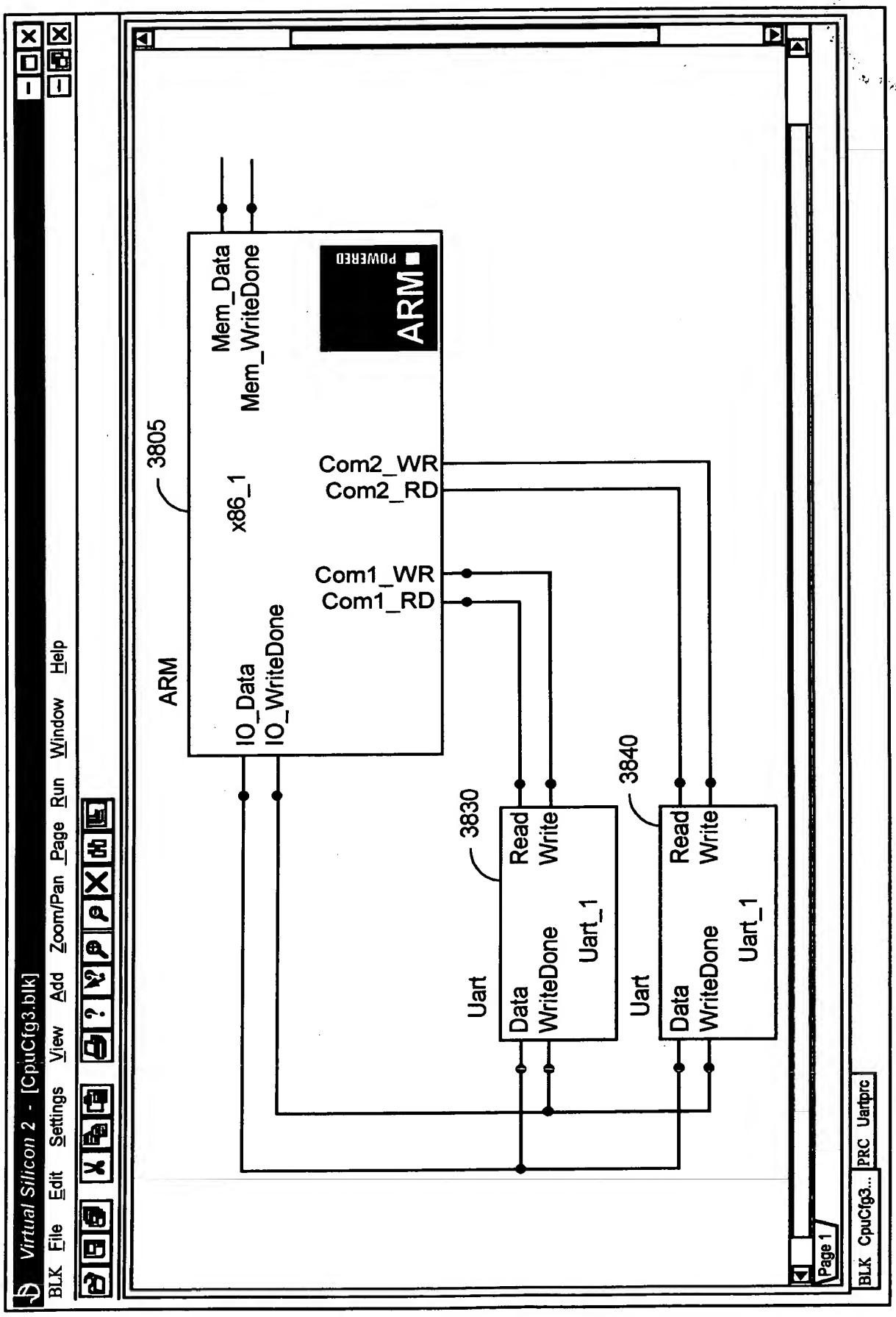

Virtual Silicon 2 - [CpuCfg3.blk]
BLK File Edit Settings View Add Zoom/Pan Page Run Window Help
POWERED
ARM
Mem_Data
Mem_WriteDone
3805
x86_1
ARM
IO_Data
IO_WriteDone
Com2_WR
Com2_RD
Com1_WR
Com1_RD
3830
Uart
Data
WriteDone
Read
Write
Uart_1
3840
Uart
Data
WriteDone
Read
Write
Uart_1
Page 1
BLK CpuCfg3...
PRC Uartprc

Figure 38

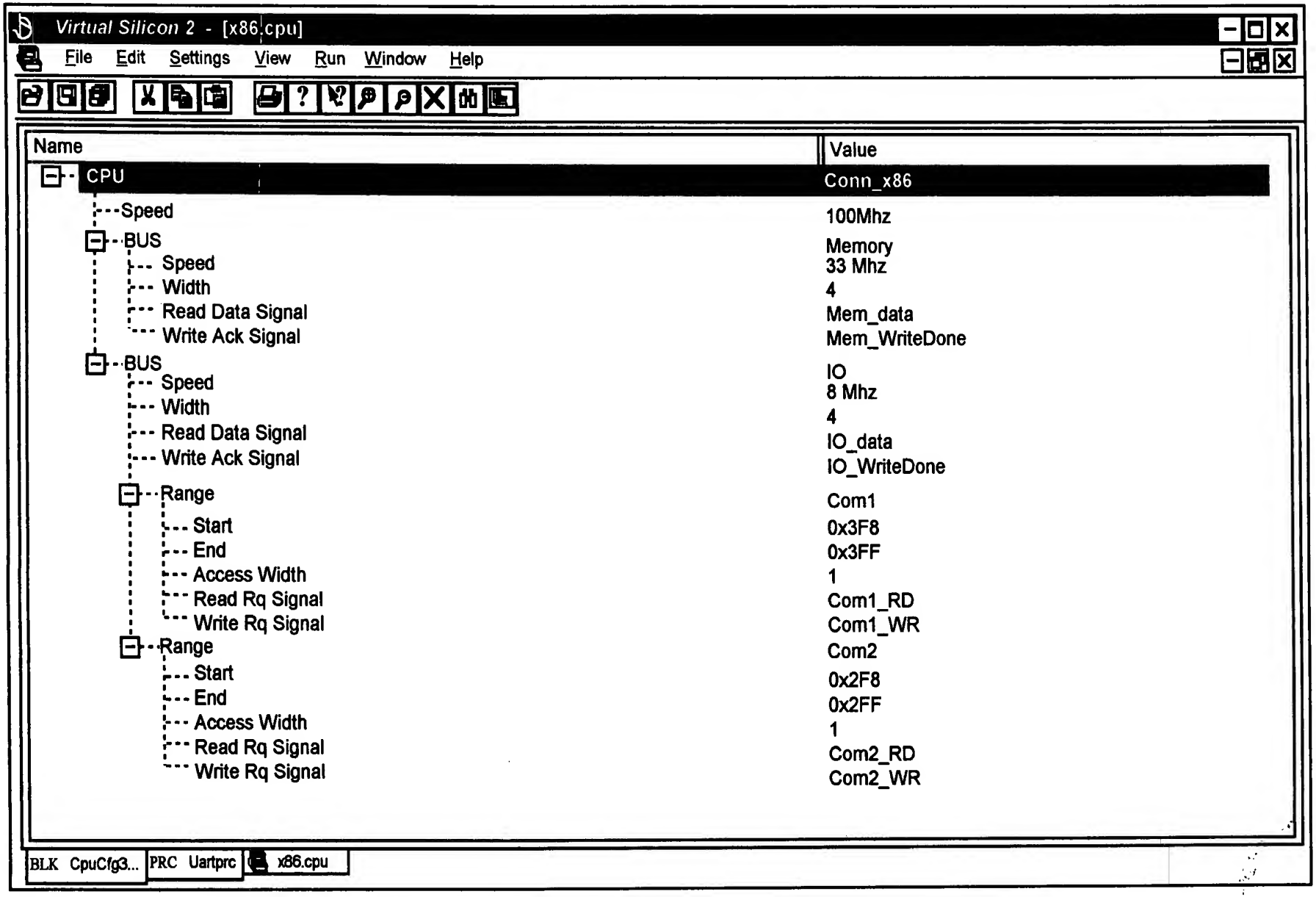


Figure 39

Application No. 09/872,435
Title: METHOD AND SYSTEM FOR VIRTUAL PROTOTYPING
Inventor(s): Stephen L. Bade et al.
Atty. Docket No.: 22178-05012
Sheet 40 of 65

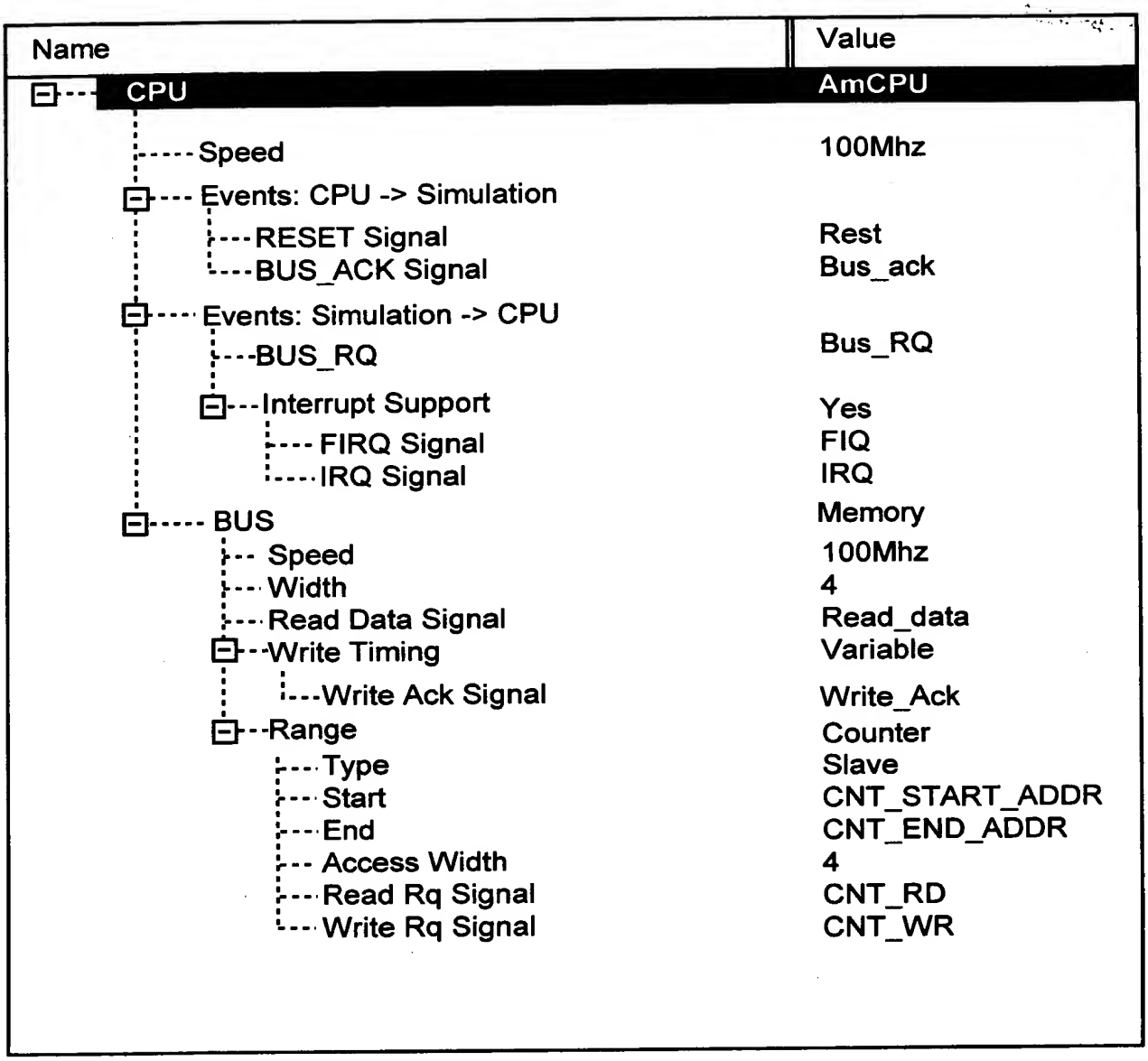

Name
Value
CPU
AmCPU
Speed
100Mhz
Events: CPU -> Simulation
RESET Signal
Rest
BUS_ACK Signal
Bus_ack
Events: Simulation -> CPU
BUS_RQ
Bus_RQ
Interrupt Support
Yes
FIRQ Signal
FIQ
IRQ Signal
IRQ
BUS
Memory
Speed
100Mhz
Width
4
Read Data Signal
Read_data
Write Timing
Variable
Write Ack Signal
Write_Ack
Range
Counter
Type
Slave
Start
CNT_START_ADDR
End
CNT_END_ADDR
Access Width
4
Read Rq Signal
CNT_RD
Write Rq Signal
CNT_WR

Figure 40

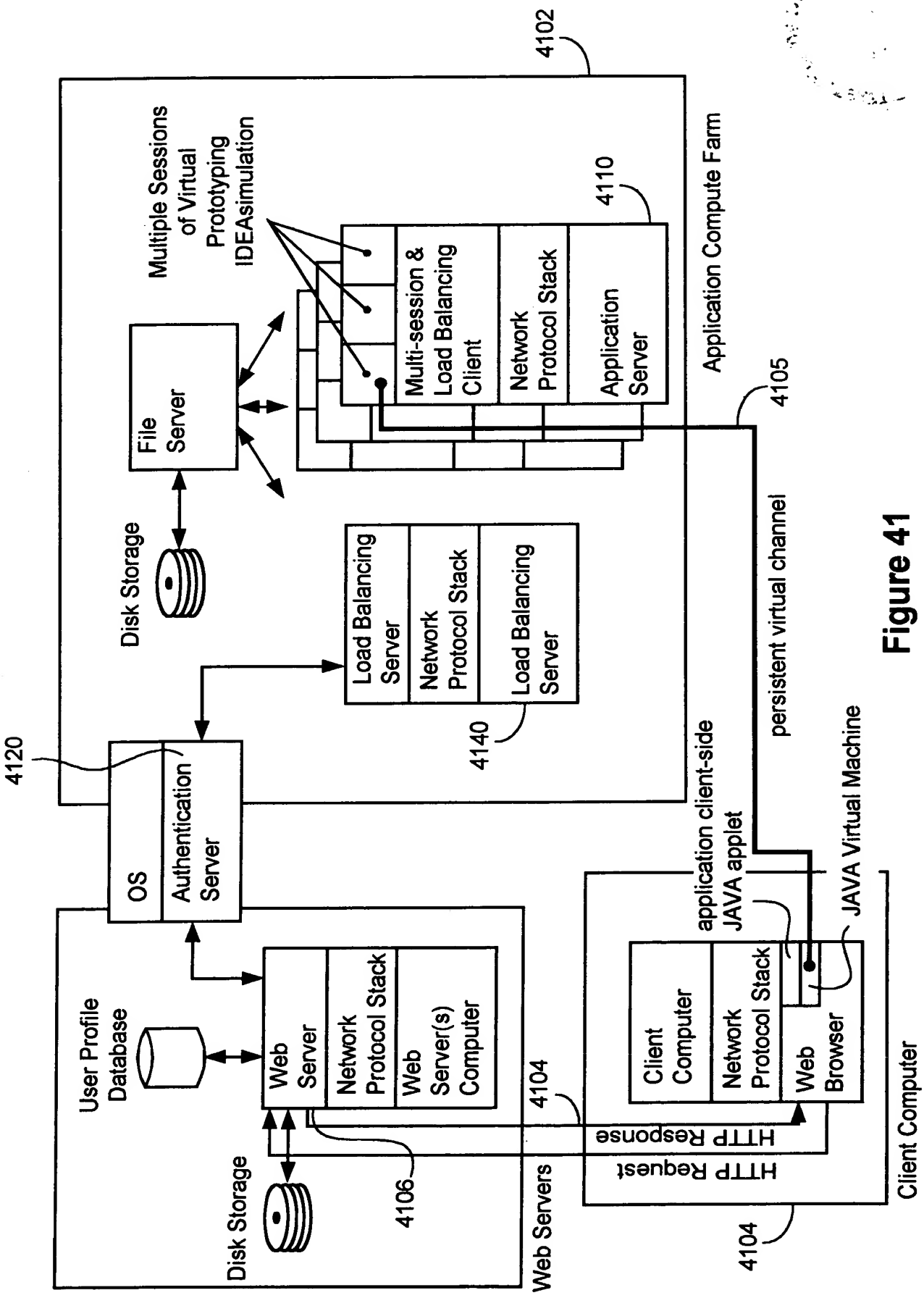
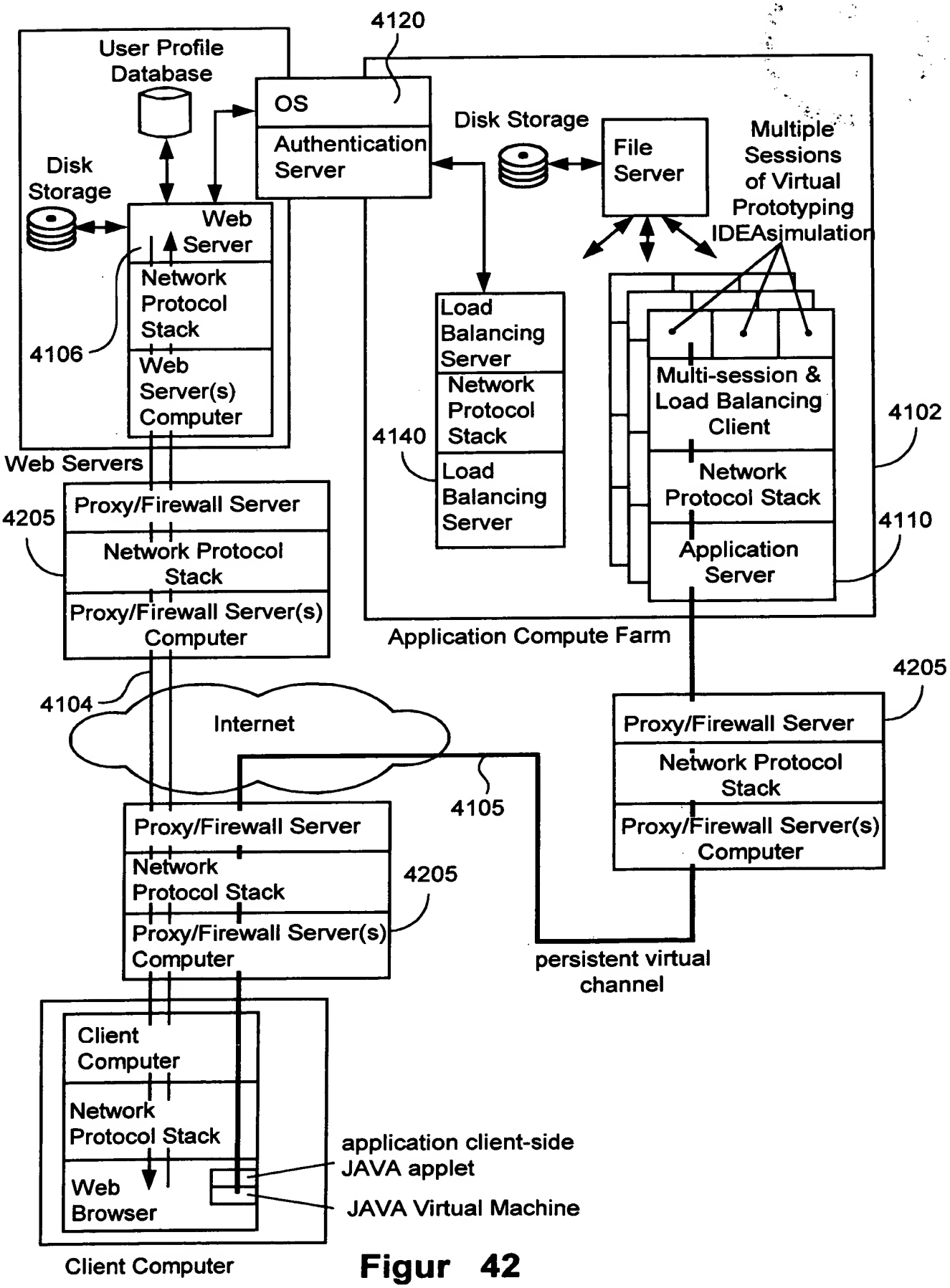

4102
Multiple Sessions of Virtual Prototyping IDEAsimulation
4110
Multi-session & Load Balancing Client
Network Protocol Stack
Application Server
Application Compute Farm
4105
File Server
Disk Storage
Load Balancing Server
Network Protocol Stack
Load Balancing Server
4140
4120
OS
Authentication Server
persistent virtual channel
application client-side JAVA applet
JAVA Virtual Machine
User Profile Database
Web Server
Network Protocol Stack
Web Server(s) Computer
4104
Client Computer
Network Protocol Stack
Web Browser
HTTP Response
HTTP Request
4106
Disk Storage
Web Servers
4104
Client Computer

Figure 41


4120
User Profile Database
OS
Authentication Server
Disk Storage
File Server
Multiple Sessions of Virtual Prototyping IDEAsimulation
Disk Storage
Web Server
Network Protocol Stack
Web Server(s) Computer
4106
Load Balancing Server
Network Protocol Stack
Load Balancing Server
4140
Multi-session & Load Balancing Client
Network Protocol Stack
Application Server
4102
4110
Web Servers
Proxy/Firewall Server
Network Protocol Stack
Proxy/Firewall Server(s) Computer
4205
Application Compute Farm
4104
Internet
4105
Proxy/Firewall Server
Network Protocol Stack
Proxy/Firewall Server(s) Computer
4205
Proxy/Firewall Server
Network Protocol Stack
Proxy/Firewall Server(s) Computer
4205
persistent virtual channel
Client Computer
Network Protocol Stack
Web Browser
application client-side JAVA applet
JAVA Virtual Machine
Client Computer

Figur 42

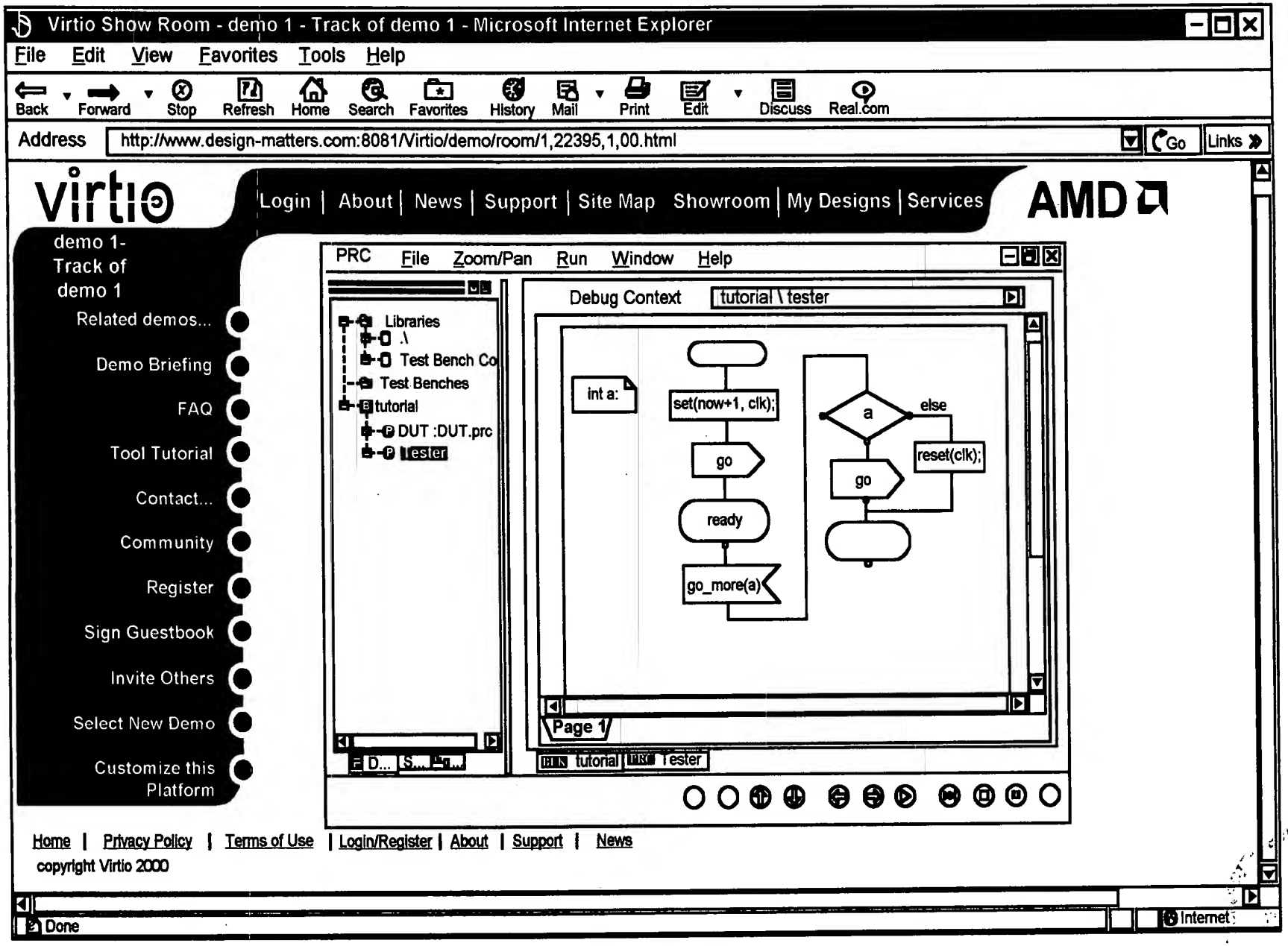


Figure 43

Application No. 09/872,435
Title: METHOD AND SYSTEM FOR VIRTUAL PROTOTYPING
Inventor(s): Stephen L. Bade et al.
Atty. Docket No.: 22178-05012
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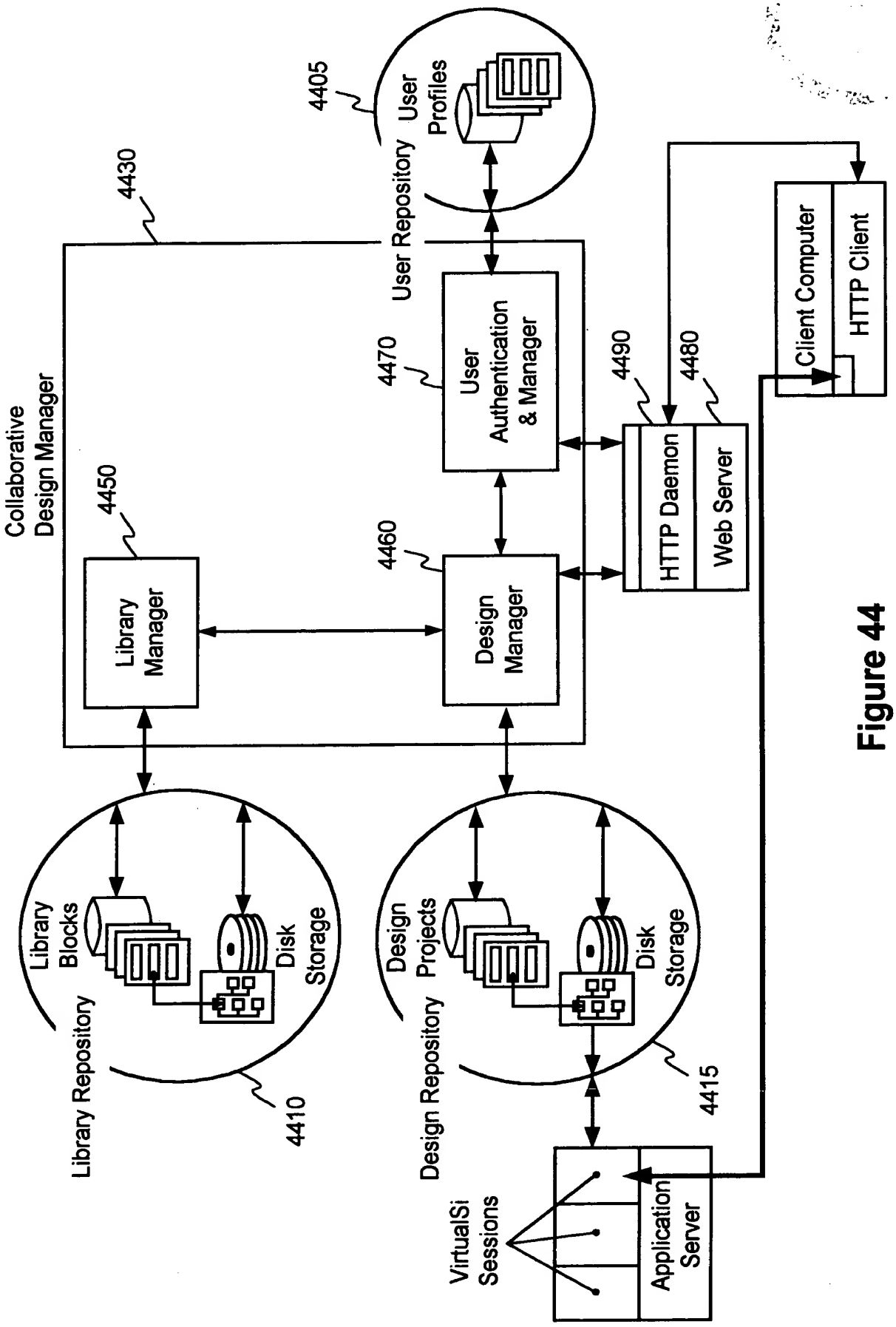

4405
User Profiles
User Repository
4430
Collaborative Design Manager
4470
User Authentication & Manager
4490
4480
Client Computer
HTTP Client
4450
Library Manager
4460
Design Manager
HTTP Daemon
Web Server
Library Blocks
Disk Storage
Library Repository
4410
Design Projects
Disk Storage
Design Repository
4415
VirtualSi Sessions
Application Server

Figure 44

{ } Clock_1	Scope Name
clk(int)	Signal name and declaration

t	Timer or clock name and declaration
S clk	Local name of a signal coming from the upper scope (inherited)
myClk	Timer or clock is being set
	Signal is being sent
	Signal is being received
	Signal is being saved

Figure 45

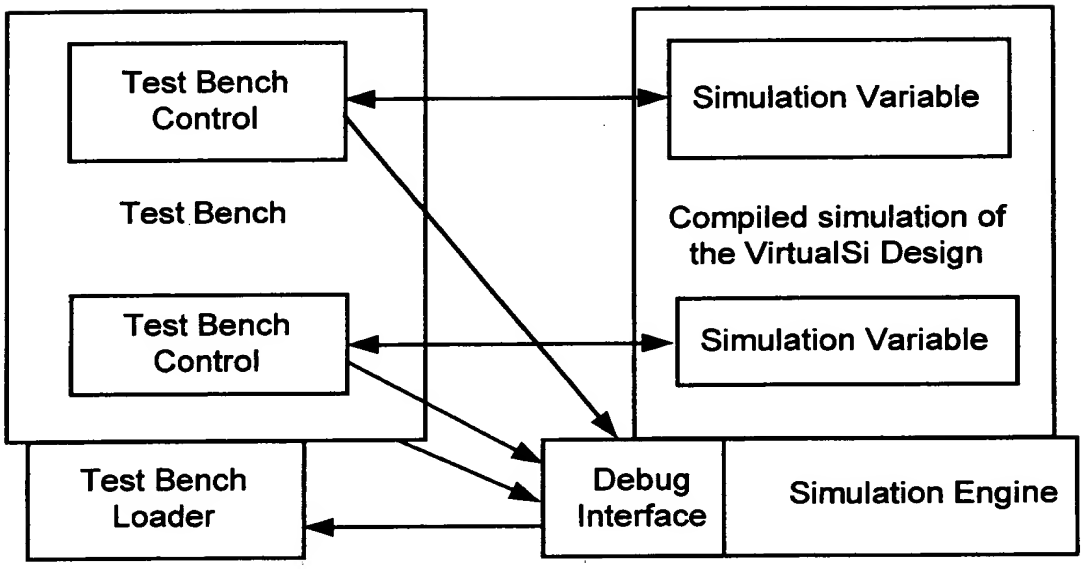

Test Bench Control
Test Bench
Test Bench Control
Test Bench Loader
Simulation Variable
Compiled simulation of the VirtualSi Design
Simulation Variable
Debug Interface
Simulation Engine

Figure 46

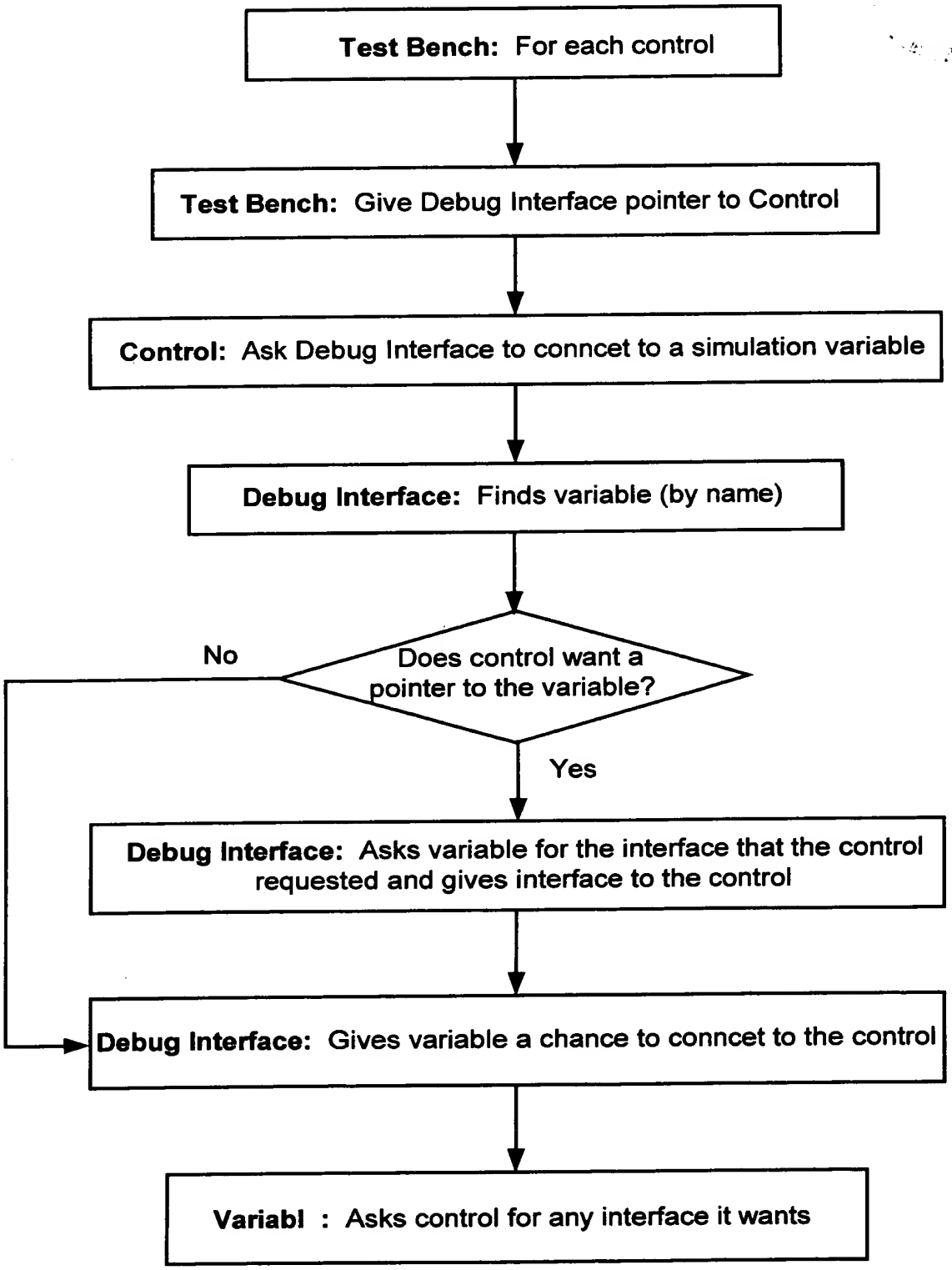

Test Bench: For each control
Test Bench: Give Debug Interface pointer to Control
Control: Ask Debug Interface to conncet to a simulation variable
Debug Interface: Finds variable (by name)
Does control want a pointer to the variable?
No
Yes
Debug Interface: Asks variable for the interface that the control requested and gives interface to the control
Debug Interface: Gives variable a chance to conncet to the control
Variabl : Asks control for any interface it wants

Figure 47

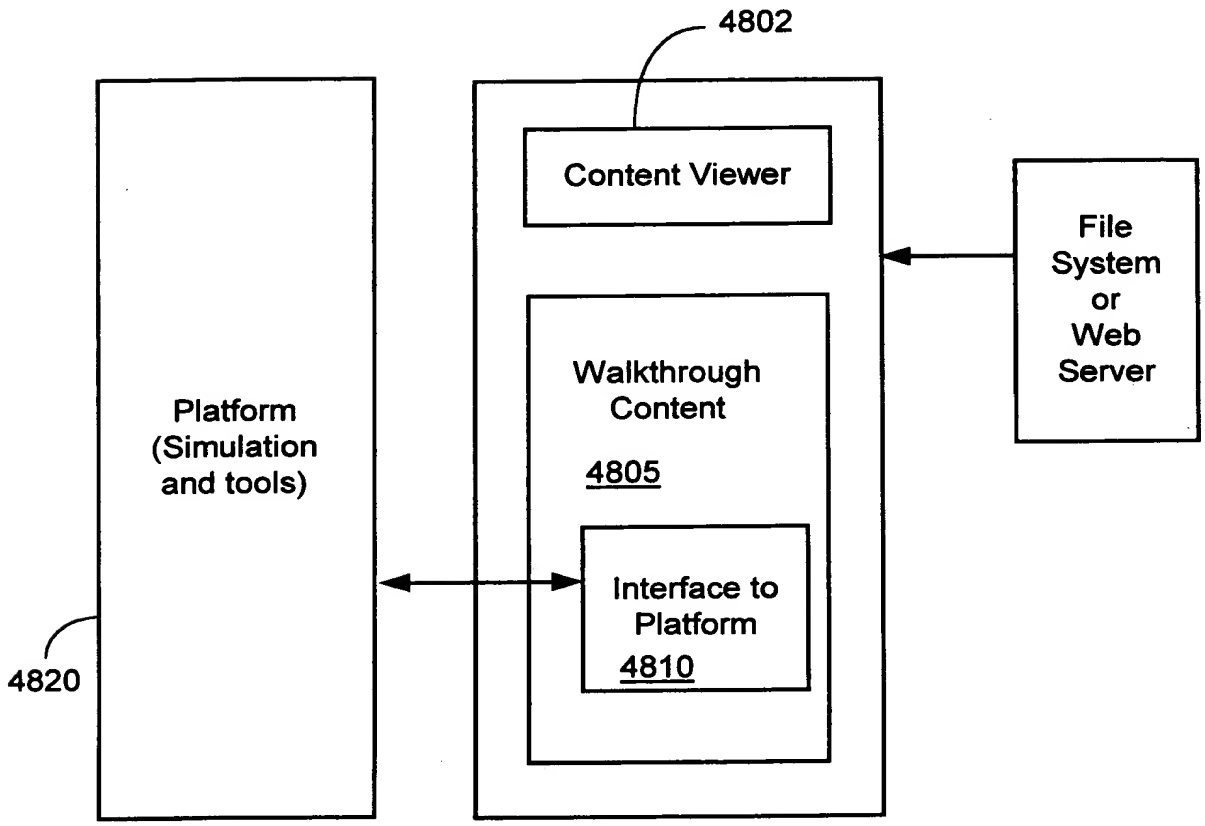

4802
Content Viewer
File System or Web Server
Walkthrough Content
4805
Platform (Simulation and tools)
Interface to Platform
4810
4820

Figure 48

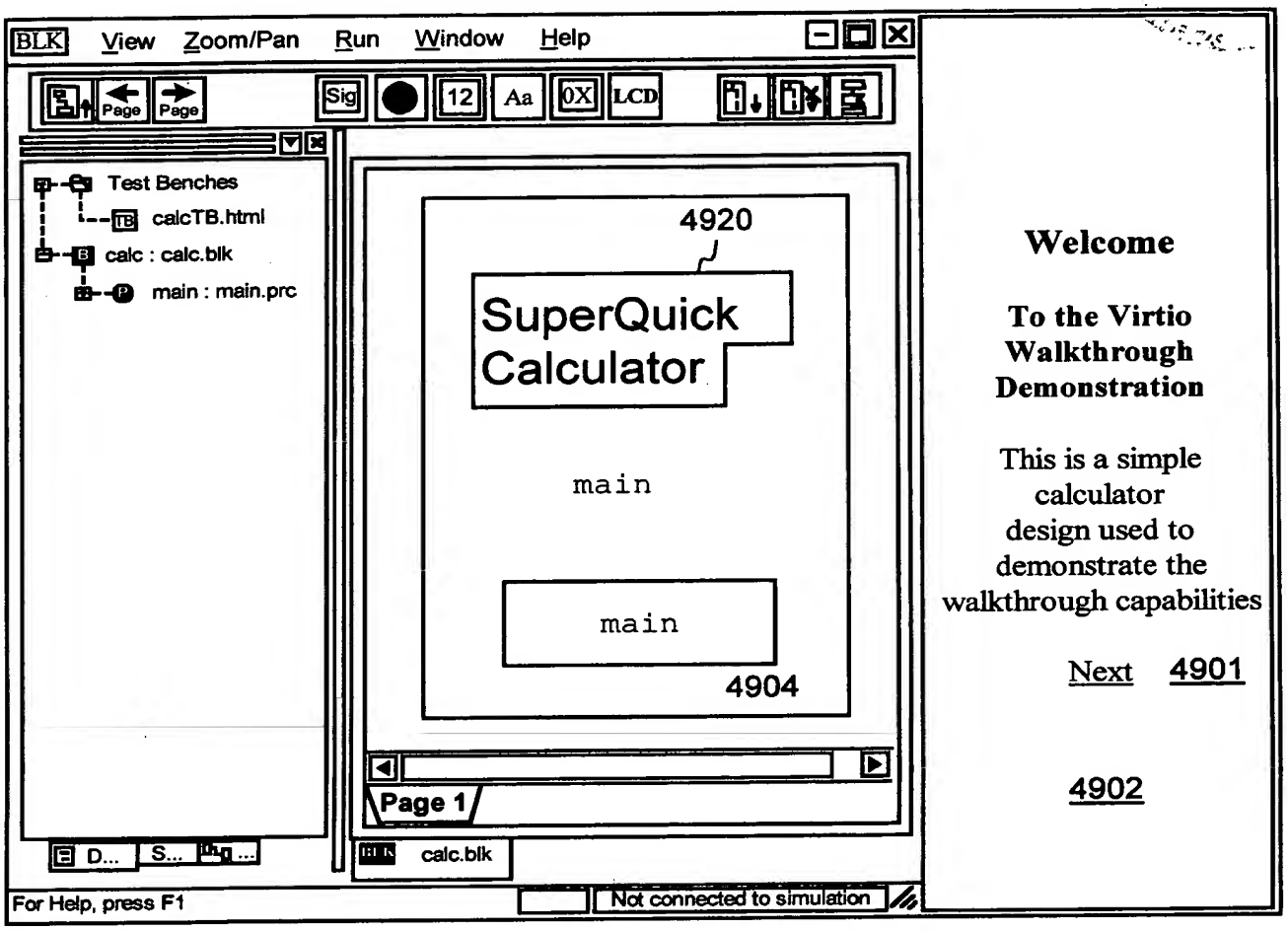

BLK
View
Zoom/Pan
Run
Window
Help
Page
Page
Sig
12
Aa
0X
LCD
Test Benches
calcTB.html
calc : calc.blk
main : main.prc
4920
SuperQuick Calculator
main
main
4904
Page 1
D...
S...
calc.blk
For Help, press F1
Not connected to simulation
Welcome
To the Virtio Walkthrough Demonstration
This is a simple calculator design used to demonstrate the walkthrough capabilities
Next 4901
4902

Figure 49A

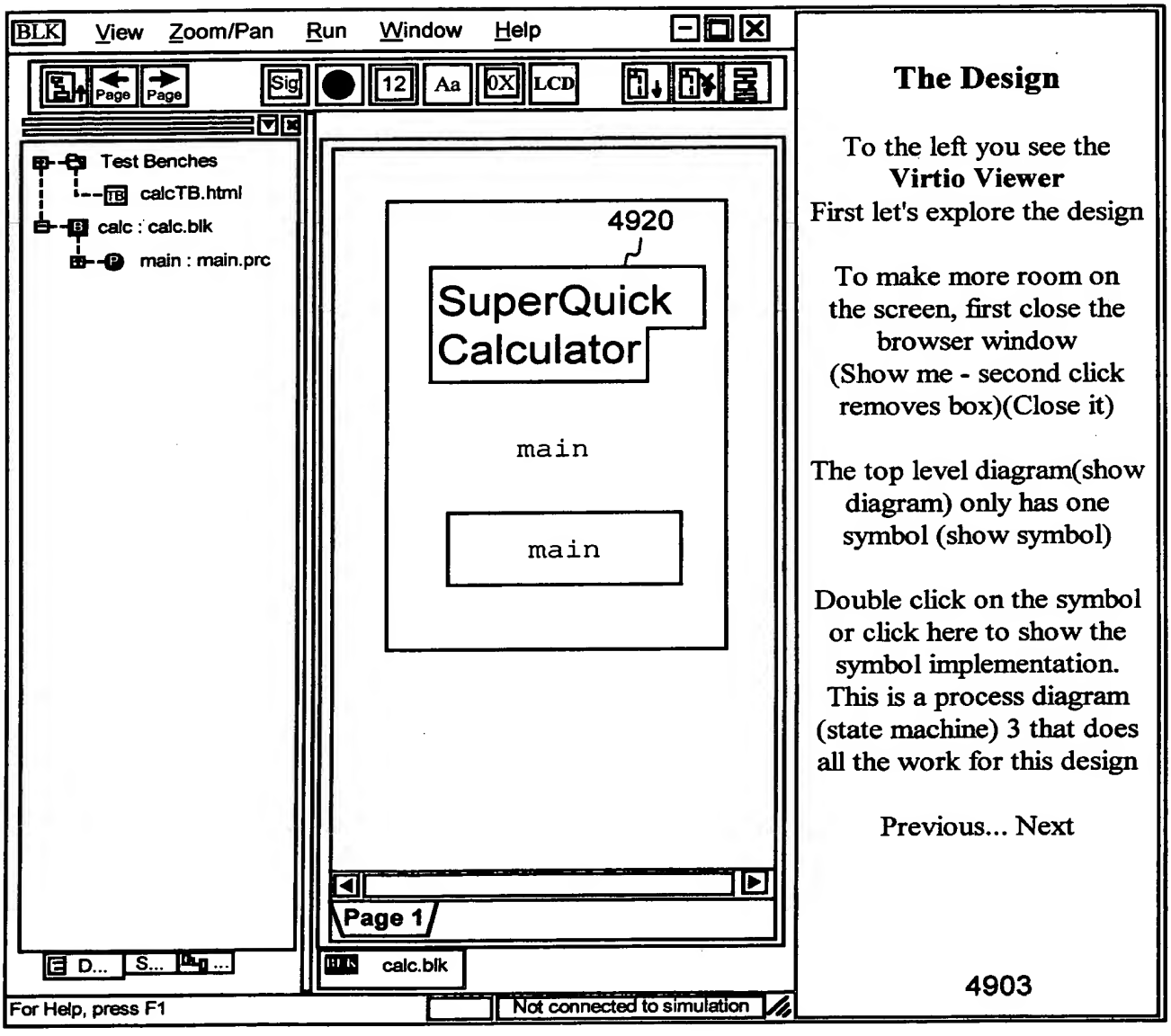

BLK
View
Zoom/Pan
Run
Window
Help
Page
Page
Sig
12
Aa
0X
LCD
Test Benches
calcTB.html
calc : calc.blk
main : main.prc
4920
SuperQuick Calculator
main
main
Page 1
calc.blk
D...
S...
For Help, press F1
Not connected to simulation
The Design
To the left you see the Virtio Viewer First let's explore the design
To make more room on the screen, first close the browser window (Show me - second click removes box)(Close it)
The top level diagram(show diagram) only has one symbol (show symbol)
Double click on the symbol or click here to show the symbol implementation. This is a process diagram (state machine) 3 that does all the work for this design
Previous... Next
4903

Figure 49B

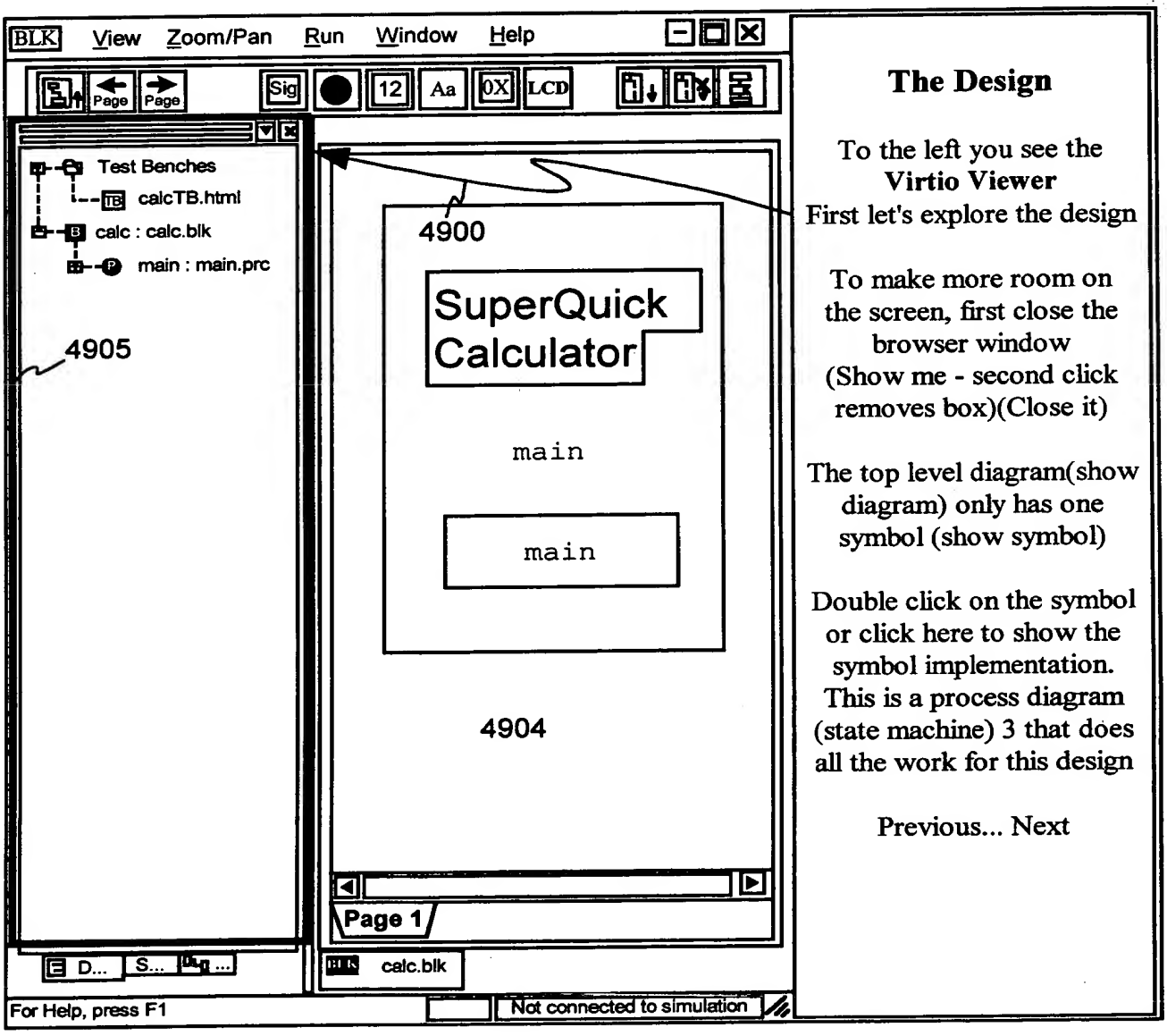
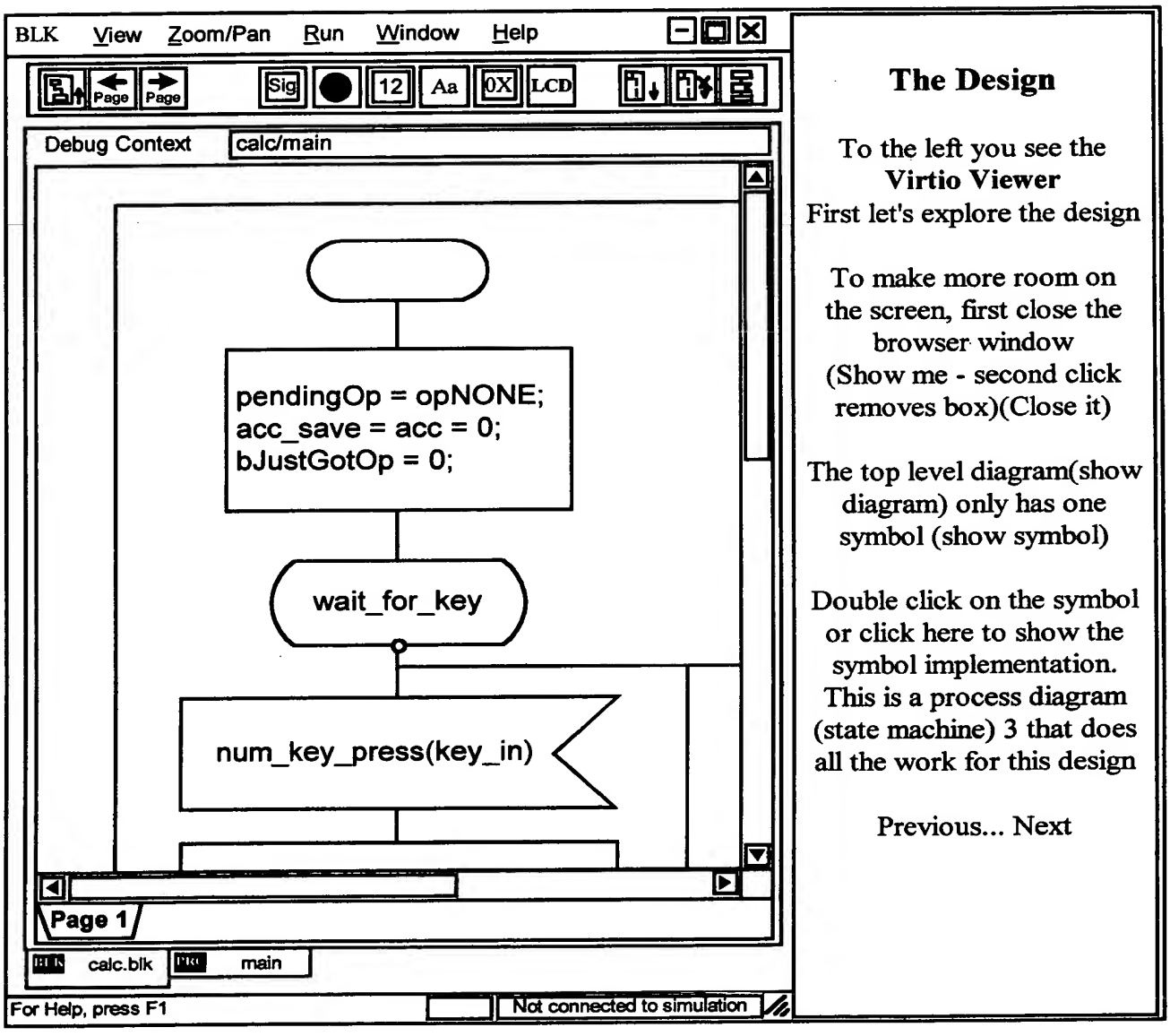

BLK
View
Zoom/Pan
Run
Window
Help
Page
Page
Sig
12
Aa
0X
LCD
Test Benches
calcTB.html
calc : calc.blk
main : main.prc
4905
4900
SuperQuick Calculator
main
main
4904
Page 1
D...
S...
calc.blk
For Help, press F1
Not connected to simulation
The Design
To the left you see the Virtio Viewer First let's explore the design
To make more room on the screen, first close the browser window (Show me - second click removes box)(Close it)
The top level diagram(show diagram) only has one symbol (show symbol)
Double click on the symbol or click here to show the symbol implementation. This is a process diagram (state machine) 3 that does all the work for this design
Previous... Next

Figure 49C


BLK View Zoom/Pan Run Window Help
Page
Page
Sig
12
Aa
0X
LCD
Debug Context
calc/main
pendingOp = opNONE;
acc_save = acc = 0;
bJustGotOp = 0;
wait_for_key
num_key_press(key_in)
Page 1
calc.blk
main
For Help, press F1
Not connected to simulation
The Design
To the left you see the Virtio Viewer First let's explore the design
To make more room on the screen, first close the browser window (Show me - second click removes box)(Close it)
The top level diagram(show diagram) only has one symbol (show symbol)
Double click on the symbol or click here to show the symbol implementation. This is a process diagram (state machine) 3 that does all the work for this design
Previous... Next

Figur 49D

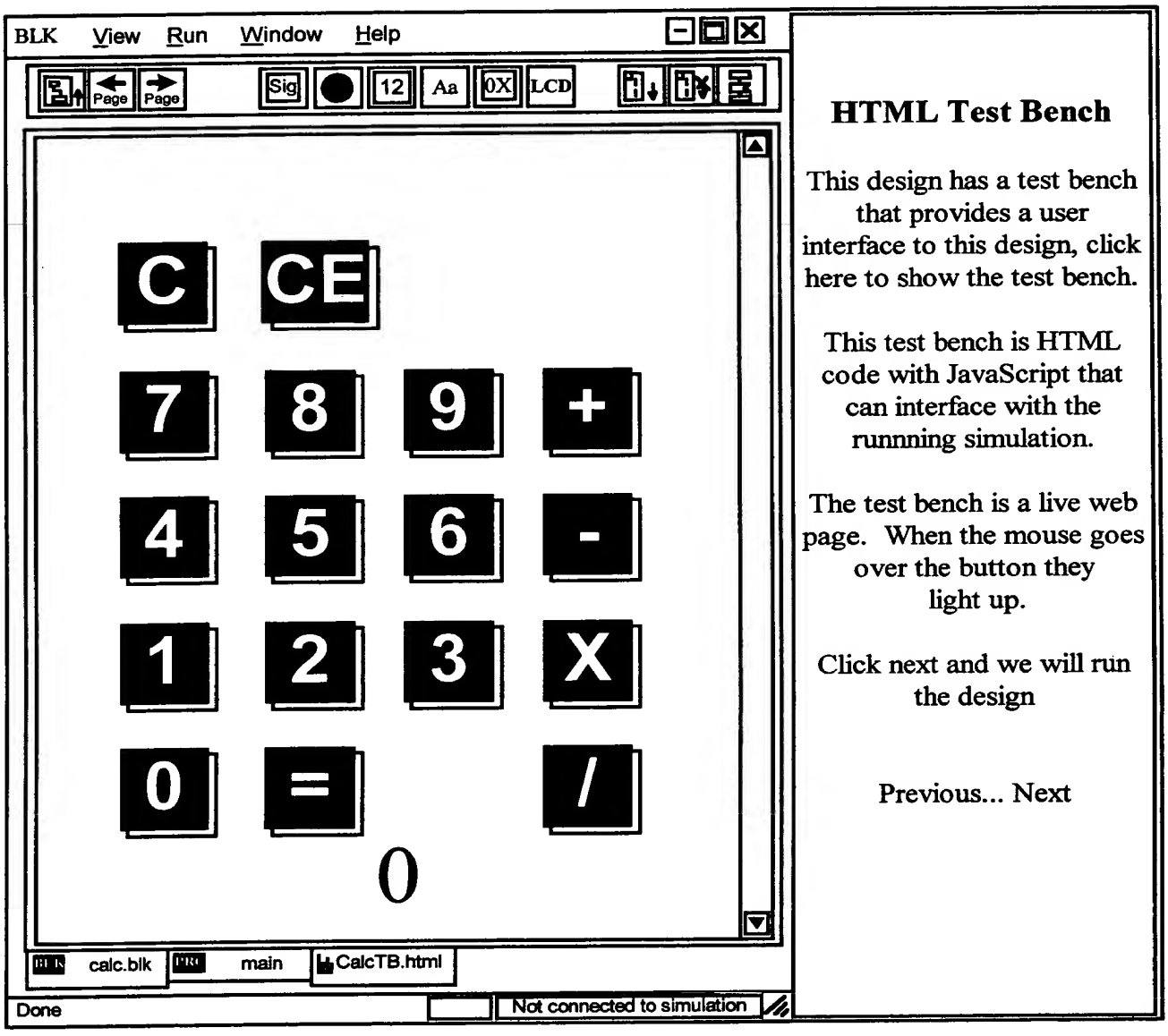
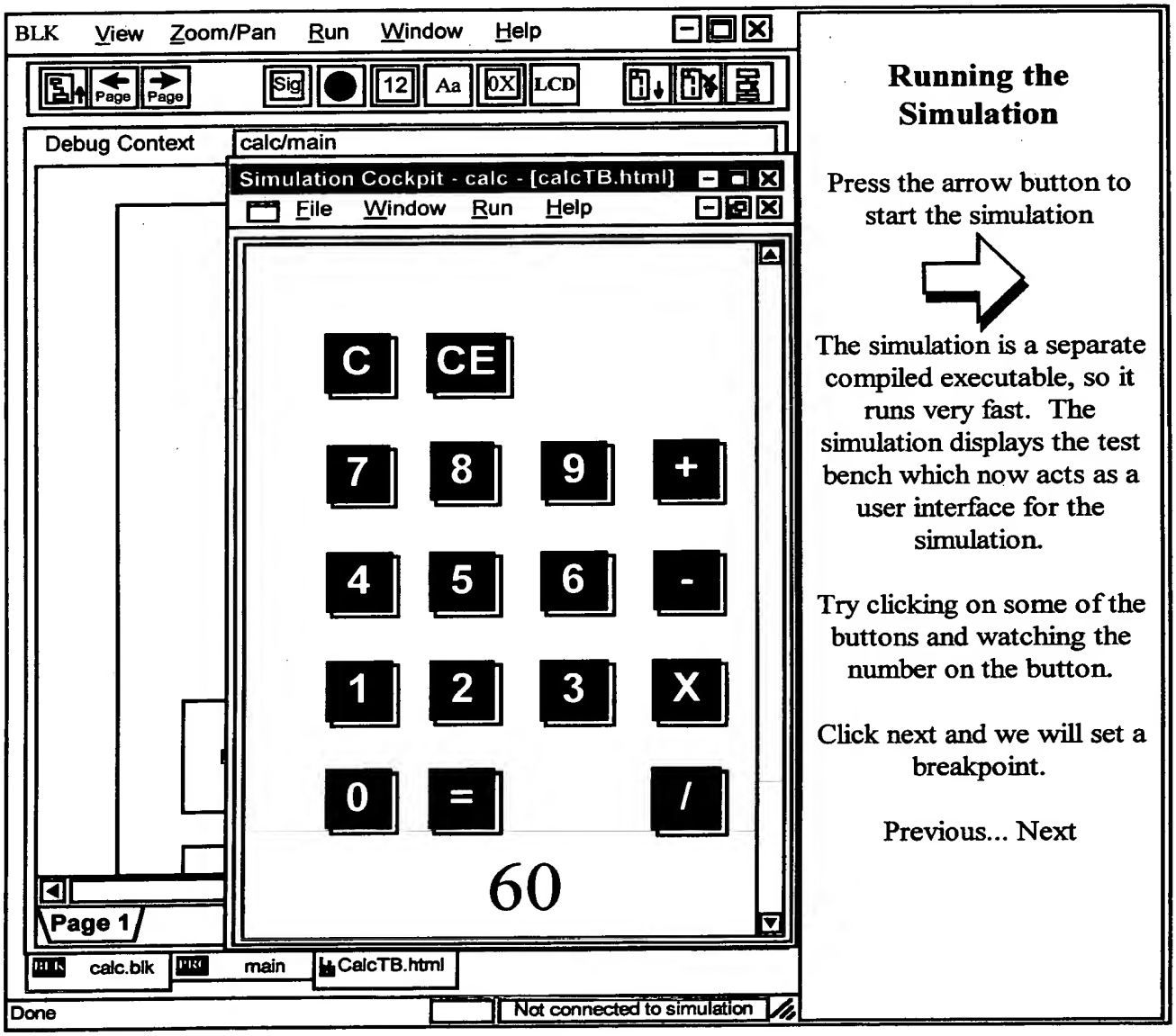
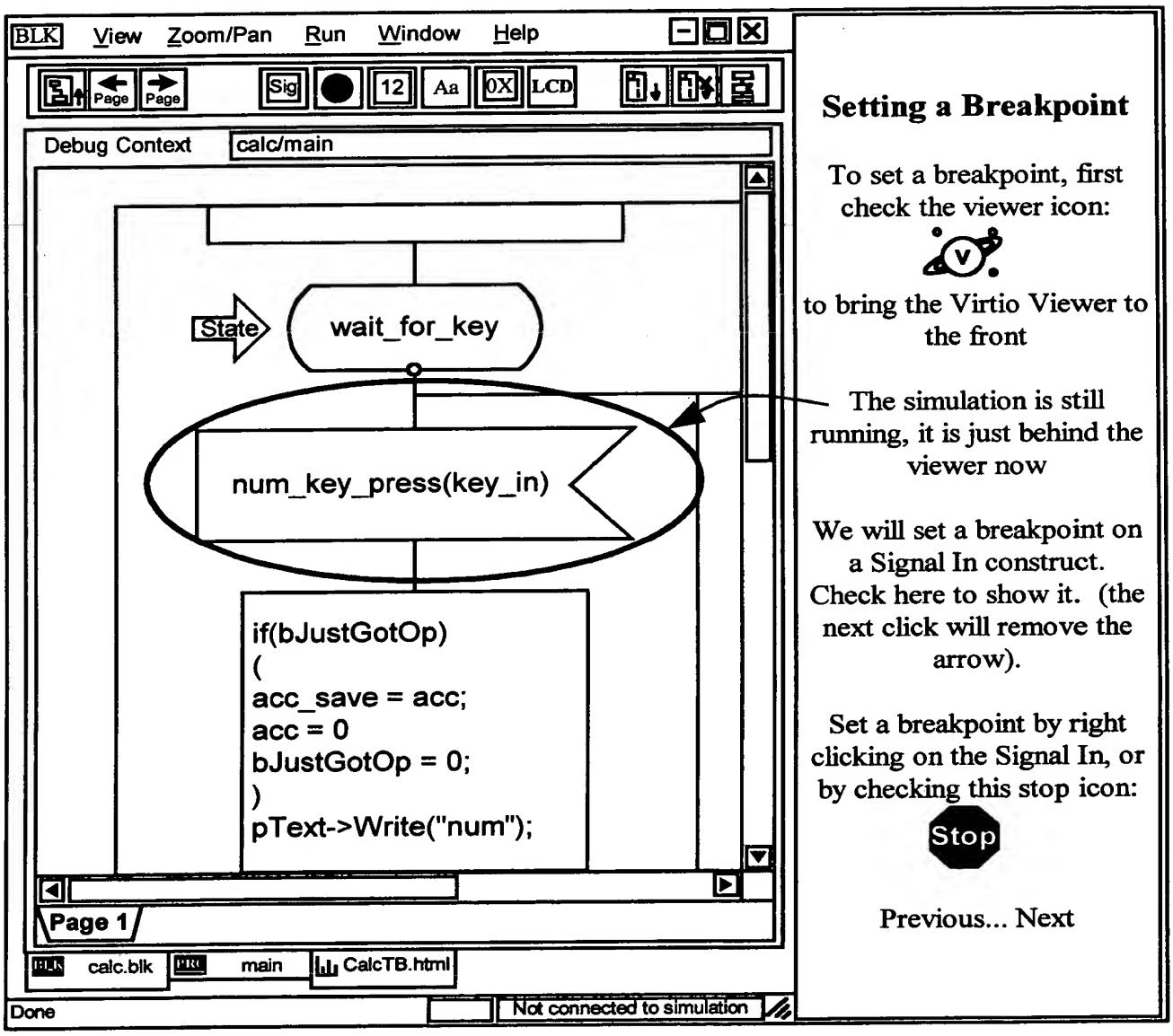

BLK View Run Window Help
Page
Page
Sig
12
Aa
0X
LCD
C
CE
7
8
9
+
4
5
6
-
1
2
3
X
0
=
/
0
calc.blk
main
CalcTB.html
Done
Not connected to simulation
HTML Test Bench
This design has a test bench that provides a user interface to this design, click here to show the test bench.
This test bench is HTML code with JavaScript that can interface with the runnning simulation.
The test bench is a live web page. When the mouse goes over the button they light up.
Click next and we will run the design
Previous... Next

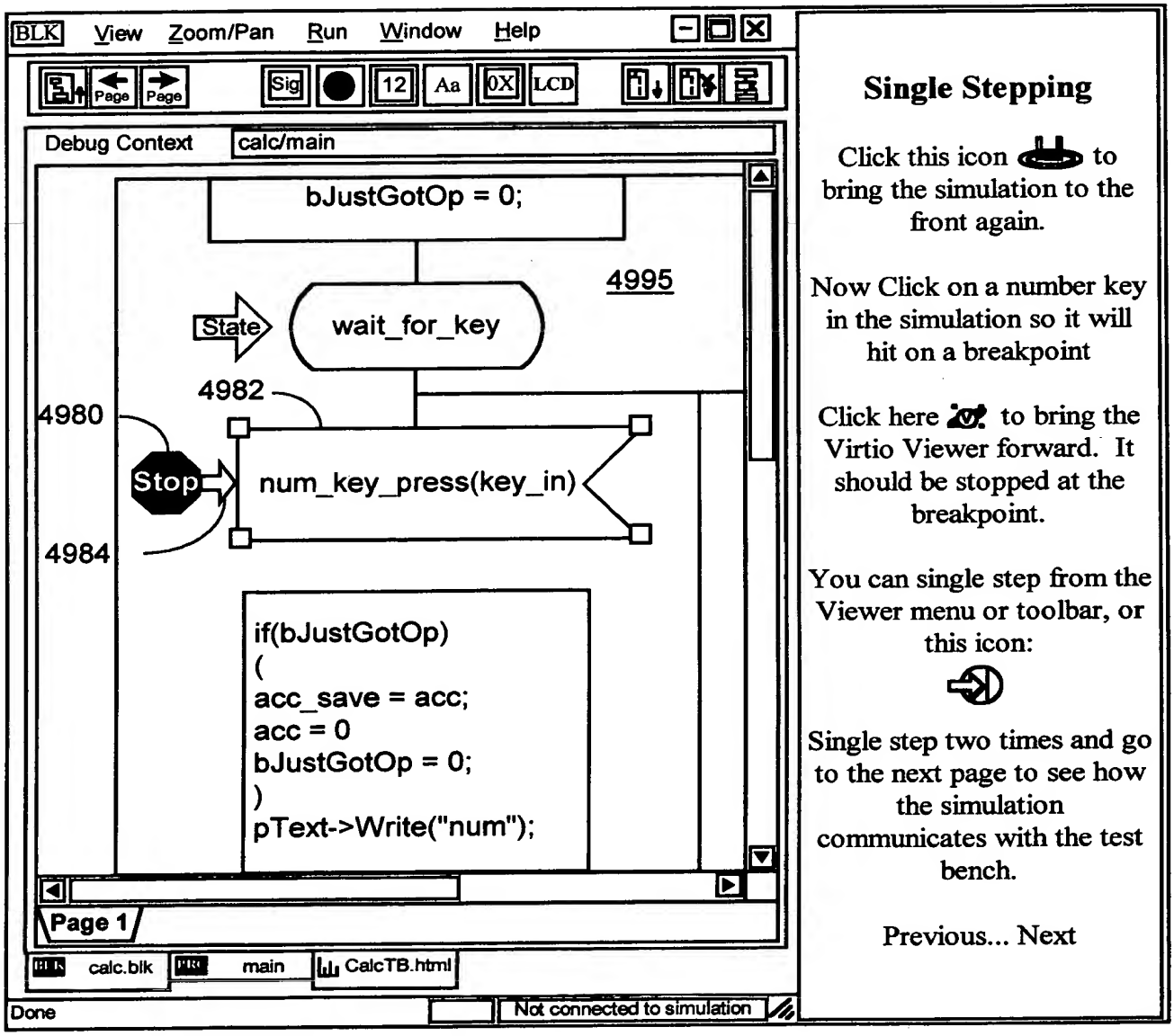
Figure 49E


BLK View Zoom/Pan Run Window Help
Page
Page
Sig
12
Aa
0X
LCD
Debug Context
calc/main
Simulation Cockpit - calc - [calcTB.html]
File Window Run Help
C
CE
7
8
9
+
4
5
6
-
1
2
3
X
0
=
/
60
Page 1
calc.blk
main
CalcTB.html
Done
Not connected to simulation
Running the Simulation
Press the arrow button to start the simulation
The simulation is a separate compiled executable, so it runs very fast. The simulation displays the test bench which now acts as a user interface for the simulation.
Try clicking on some of the buttons and watching the number on the button.
Click next and we will set a breakpoint.
Previous... Next

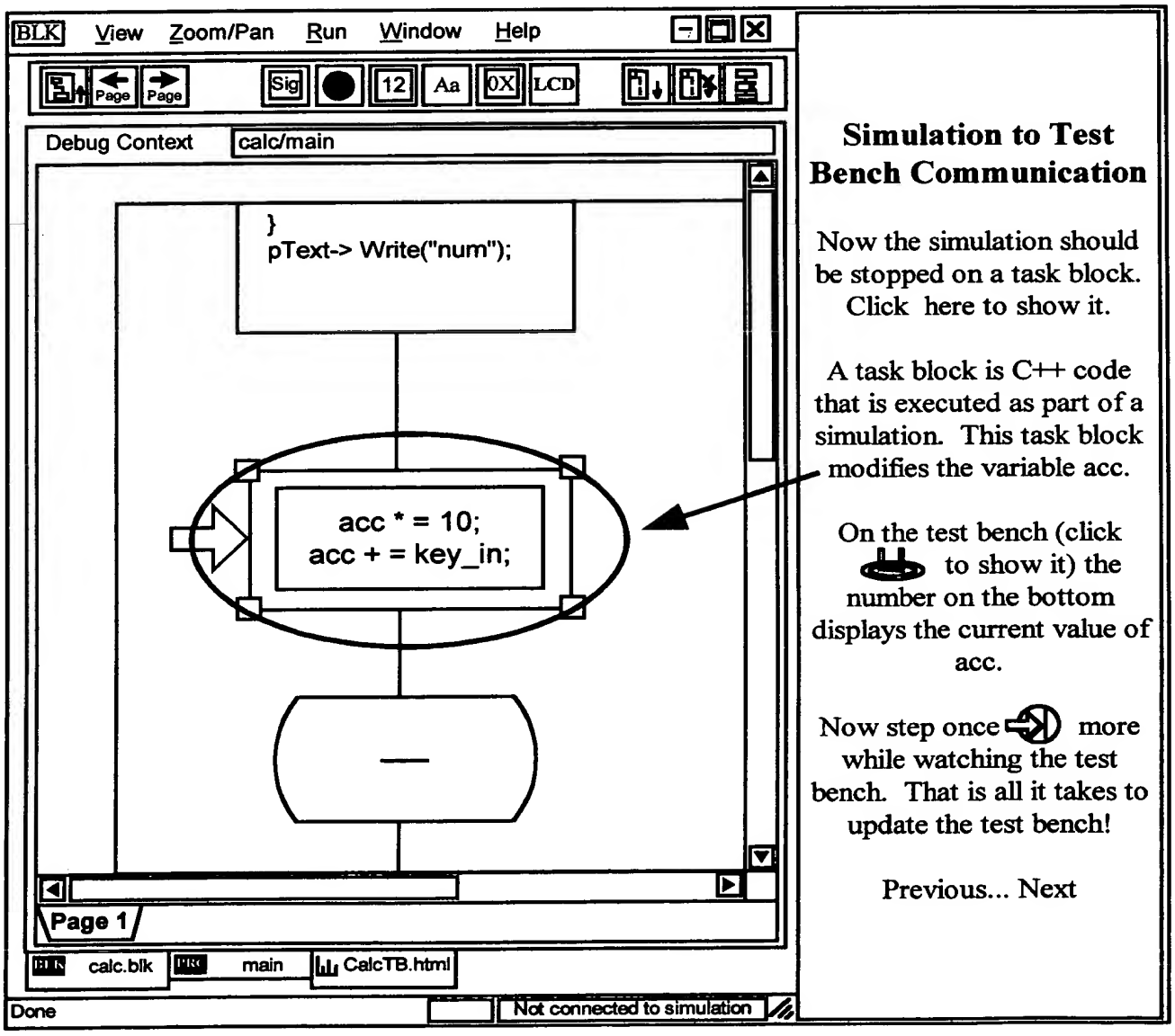
Figur 49F


BLK
View
Zoom/Pan
Run
Window
Help
Page
Page
Sig
12
Aa
0X
LCD
Debug Context
calc/main
State
wait_for_key
num_key_press(key_in)
if(bJustGotOp)
(
acc_save = acc;
acc = 0
bJustGotOp = 0;
)
pText->Write("num");
Page 1
calc.blk
main
CalcTB.html
Done
Not connected to simulation
Setting a Breakpoint
To set a breakpoint, first check the viewer icon:
to bring the Virtio Viewer to the front
The simulation is still running, it is just behind the viewer now
We will set a breakpoint on a Signal In construct. Check here to show it. (the next click will remove the arrow).
Set a breakpoint by right clicking on the Signal In, or by checking this stop icon:
Stop
Previous... Next

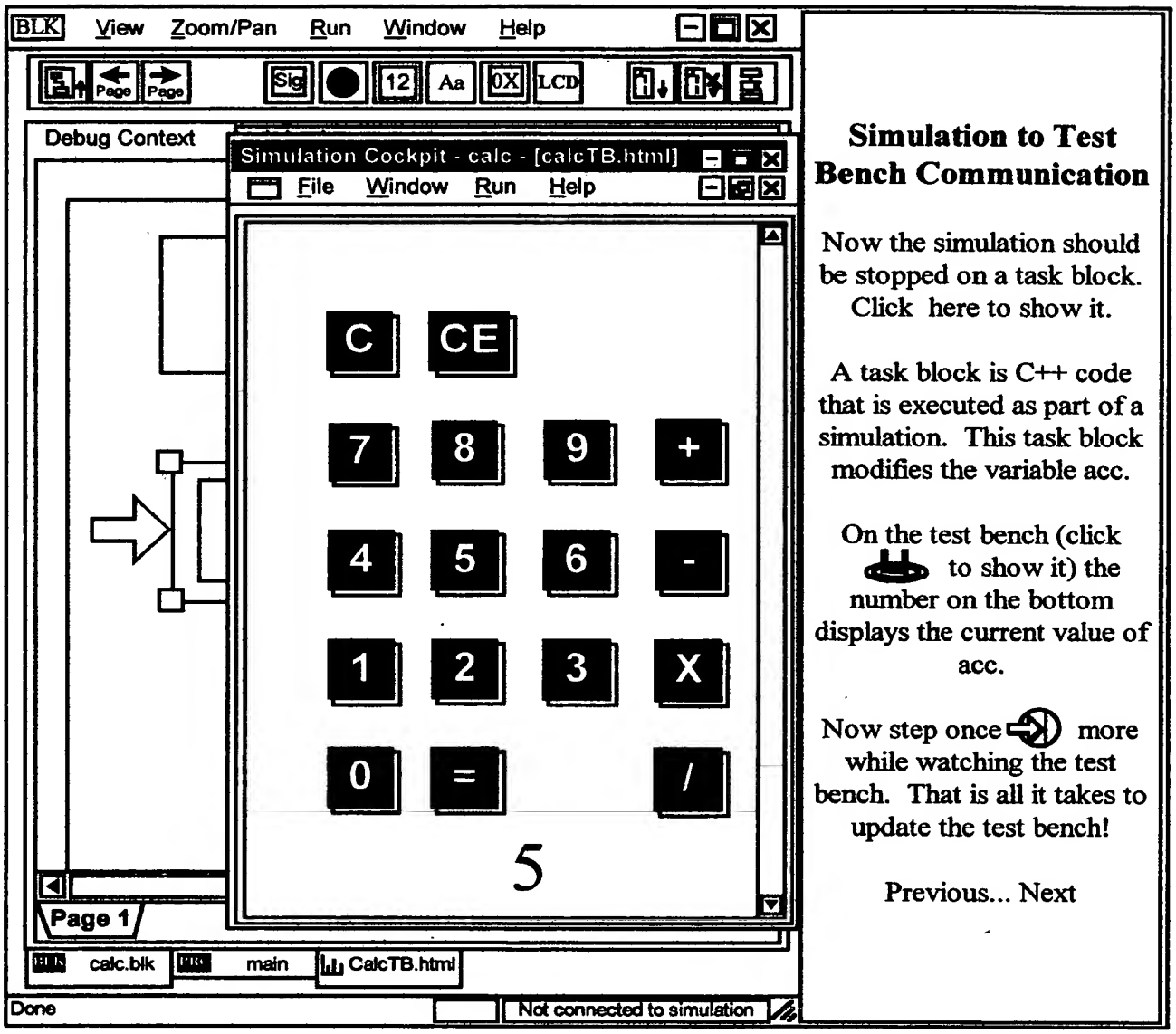
Figur 49G


BLK
View
Zoom/Pan
Run
Window
Help
Page
Page
Sig
12
Aa
0X
LCD
Debug Context
calc/main
bJustGotOp = 0;
4995
State
wait_for_key
4982
4980
Stop
num_key_press(key_in)
4984
if(bJustGotOp)
(
acc_save = acc;
acc = 0
bJustGotOp = 0;
)
pText->Write("num");
Page 1
calc.blk
main
CalcTB.html
Done
Not connected to simulation
Single Stepping
Click this icon to bring the simulation to the front again.
Now Click on a number key in the simulation so it will hit on a breakpoint
Click here to bring the Virtio Viewer forward. It should be stopped at the breakpoint.
You can single step from the Viewer menu or toolbar, or this icon:
Single step two times and go to the next page to see how the simulation communicates with the test bench.
Previous... Next

Figur 49H


BLK
View
Zoom/Pan
Run
Window
Help
Page
Page
Sig
12
Aa
0X
LCD
Debug Context
calc/main
}
pText-> Write("num");
acc * = 10;
acc + = key_in;
Page 1
calc.blk
main
CalcTB.html
Done
Not connected to simulation
Simulation to Test Bench Communication
Now the simulation should be stopped on a task block. Click here to show it.
A task block is C++ code that is executed as part of a simulation. This task block modifies the variable acc.
On the test bench (click to show it) the number on the bottom displays the current value of acc.
Now step once more while watching the test bench. That is all it takes to update the test bench!
Previous... Next

Figur 49l


BLK View Zoom/Pan Run Window Help
Page Page
Sig 12 Aa 0X LCD
Debug Context
Simulation Cockpit - calc - [calcTB.html]
File Window Run Help
C CE
7 8 9 +
4 5 6 -
1 2 3 X
0 = /
5
Page 1
calc.blk main CalcTB.html
Done
Not connected to simulation
Simulation to Test Bench Communication
Now the simulation should be stopped on a task block. Click here to show it.
A task block is C++ code that is executed as part of a simulation. This task block modifies the variable acc.
On the test bench (click to show it) the number on the bottom displays the current value of acc.
Now step once more while watching the test bench. That is all it takes to update the test bench!
Previous... Next

Figur 49J

Integrator Lab Screen Snap Shots - On-Line Enablement

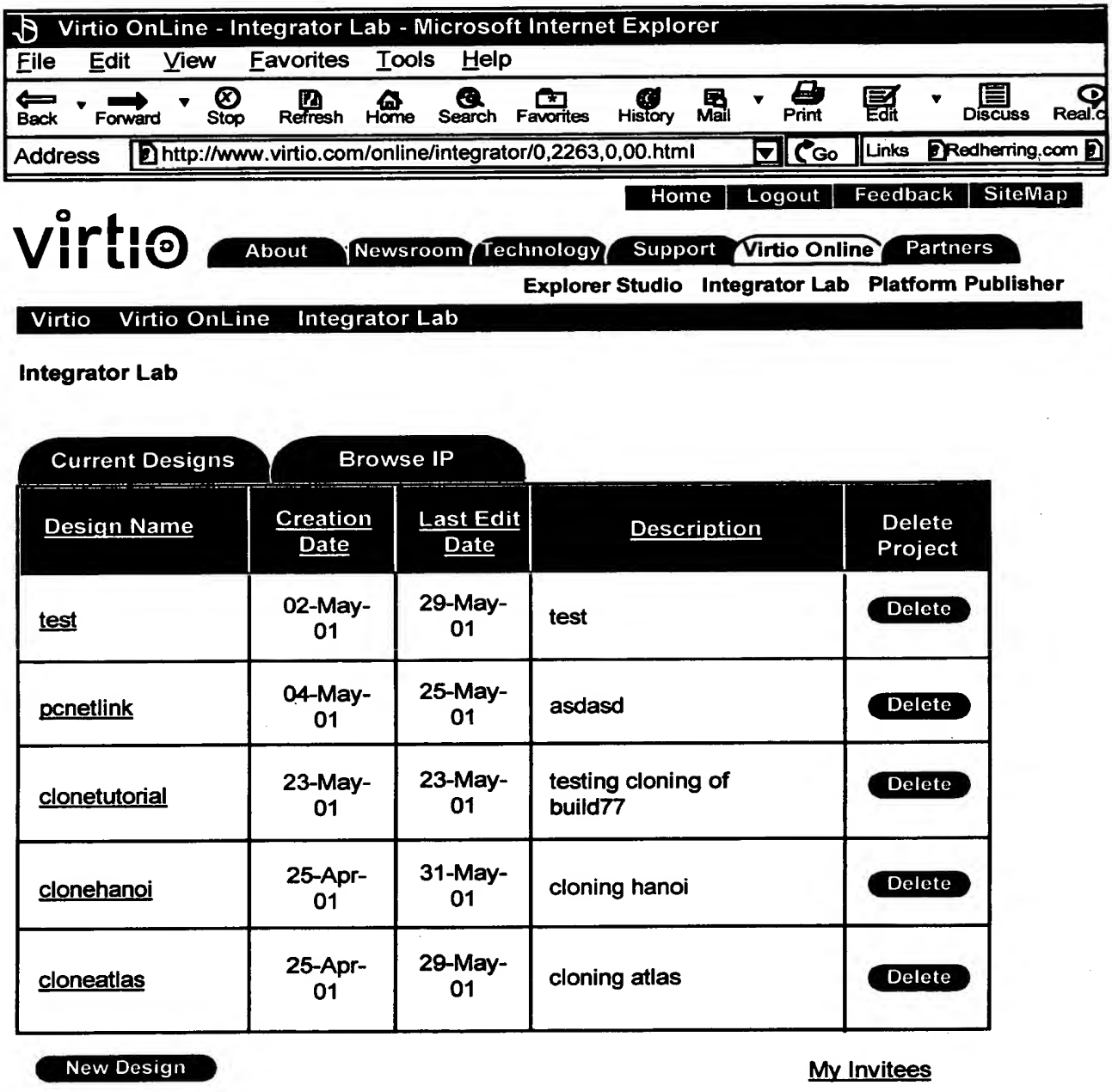


Figure 50

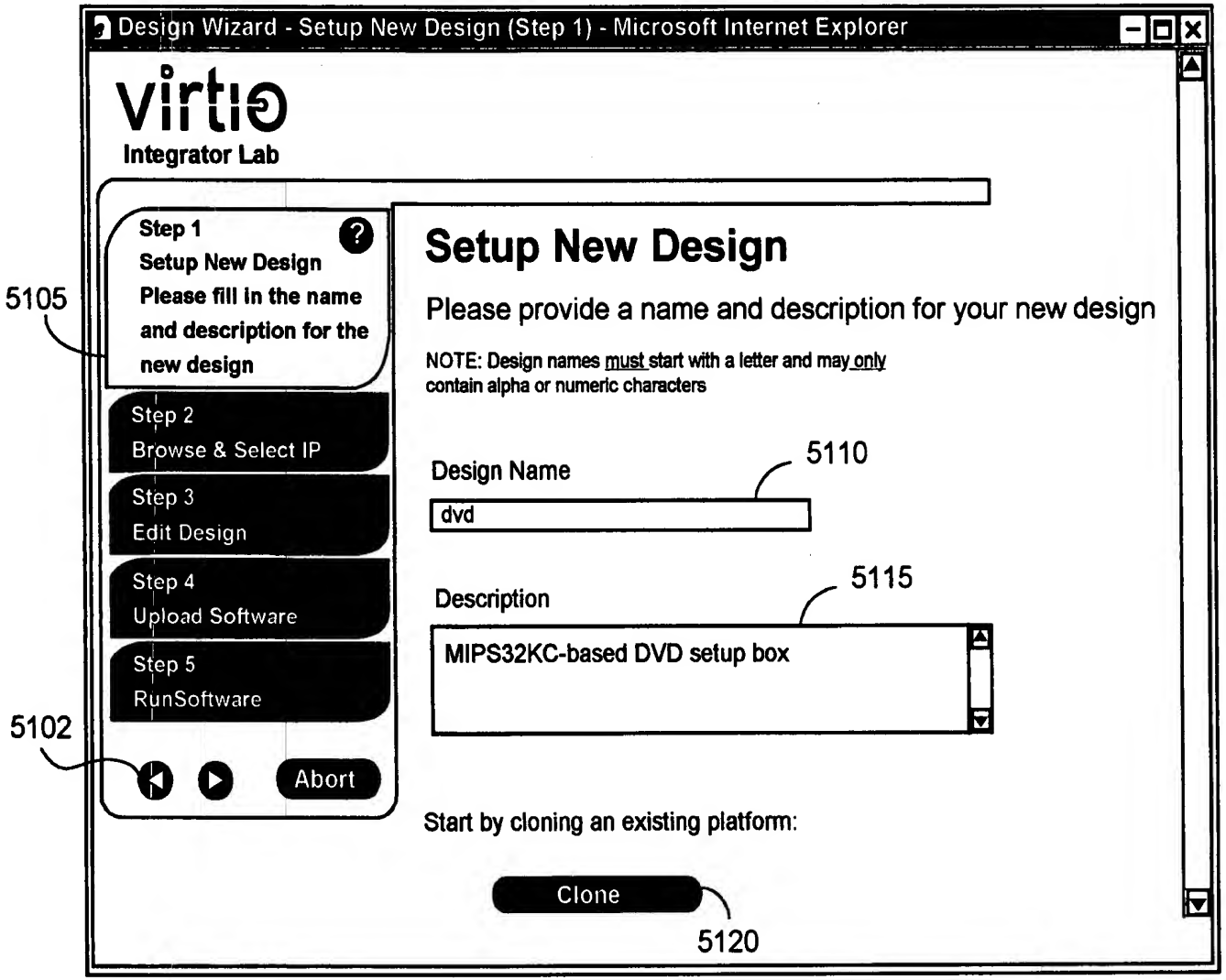


Figure 51

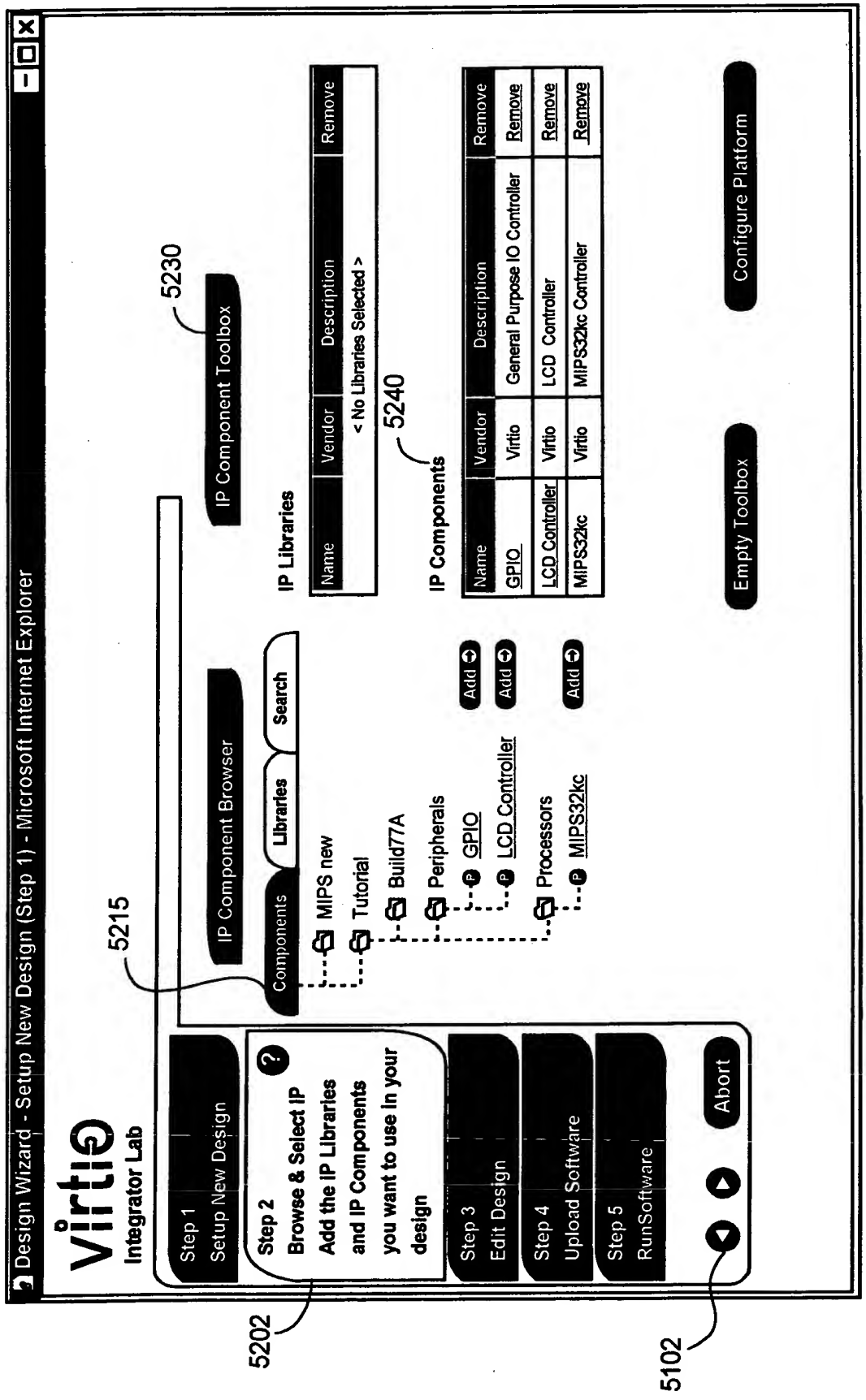

Design Wizard - Setup New Design (Step 1) - Microsoft Internet Explorer
virtio
Integrator Lab
Step 1
Setup New Design
Step 2
Browse & Select IP
Add the IP Libraries
and IP Components
you want to use in your
design
Step 3
Edit Design
Step 4
Upload Software
Step 5
RunSoftware
Abort
5215
IP Component Browser
Components
Libraries
Search
MIPS new
Tutorial
Build77A
Peripherals
GPIO
LCD Controller
Processors
MIPS32kc
Add
Add
Add
5230
IP Component Toolbox
IP Libraries
Name
Vendor
Description
Remove
< No Libraries Selected >
5240
IP Components
Name
Vendor
Description
Remove
GPIO
Virtio
General Purpose IO Controller
Remove
LCD Controller
Virtio
LCD Controller
Remove
MIPS32kc
Virtio
MIPS32kc Controller
Remove
Empty Toolbox
Configure Platform
5202
5102

Figure 52

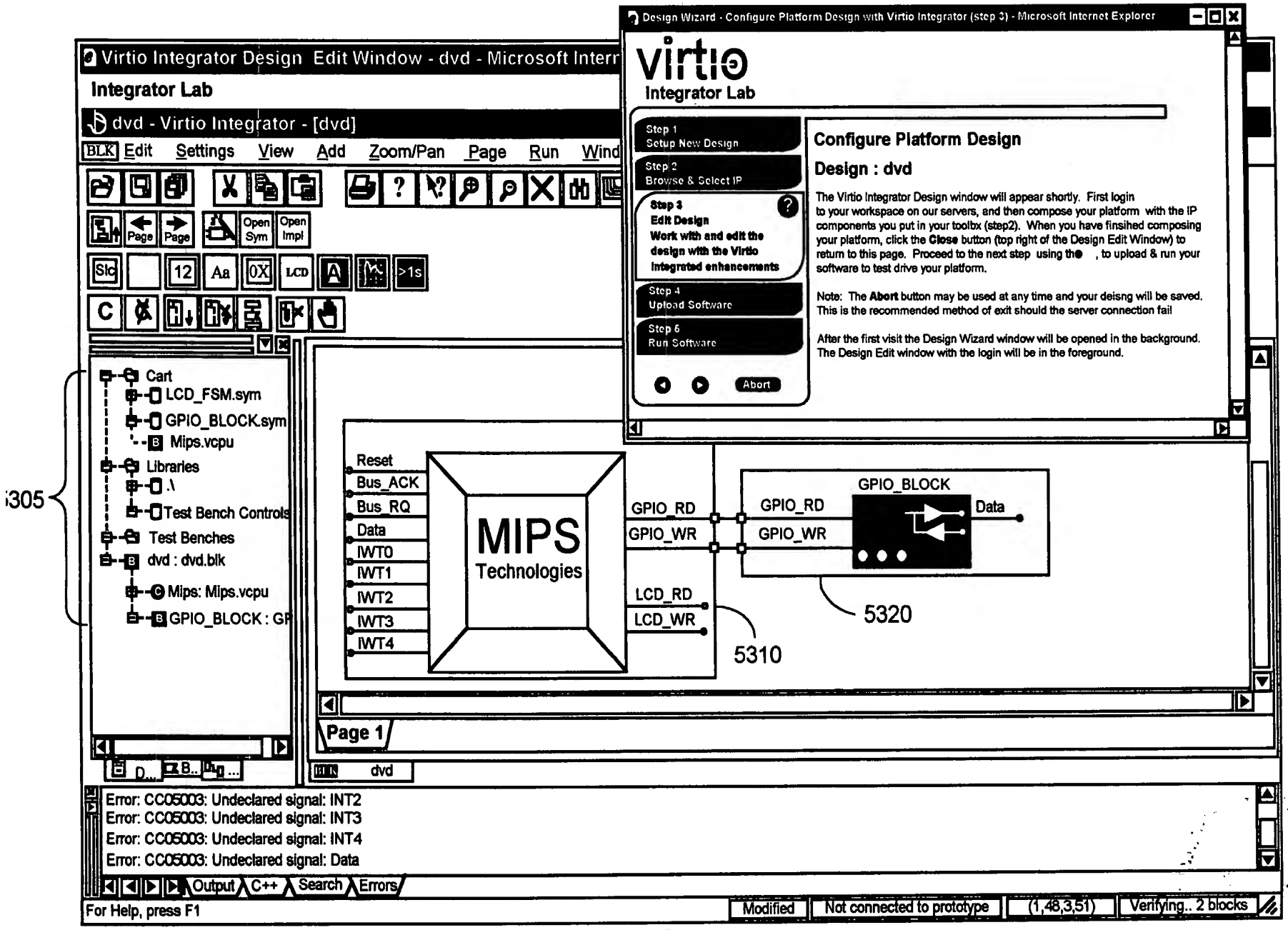


Figure 53

Application No. 09/872,435
Title: METHOD AND SYSTEM FOR VIRTUAL PROTOTYPING
Inventor(s): Stephen L. Bade et al.
Atty. Docket No.: 22178-05012
Sheet 63 of 65

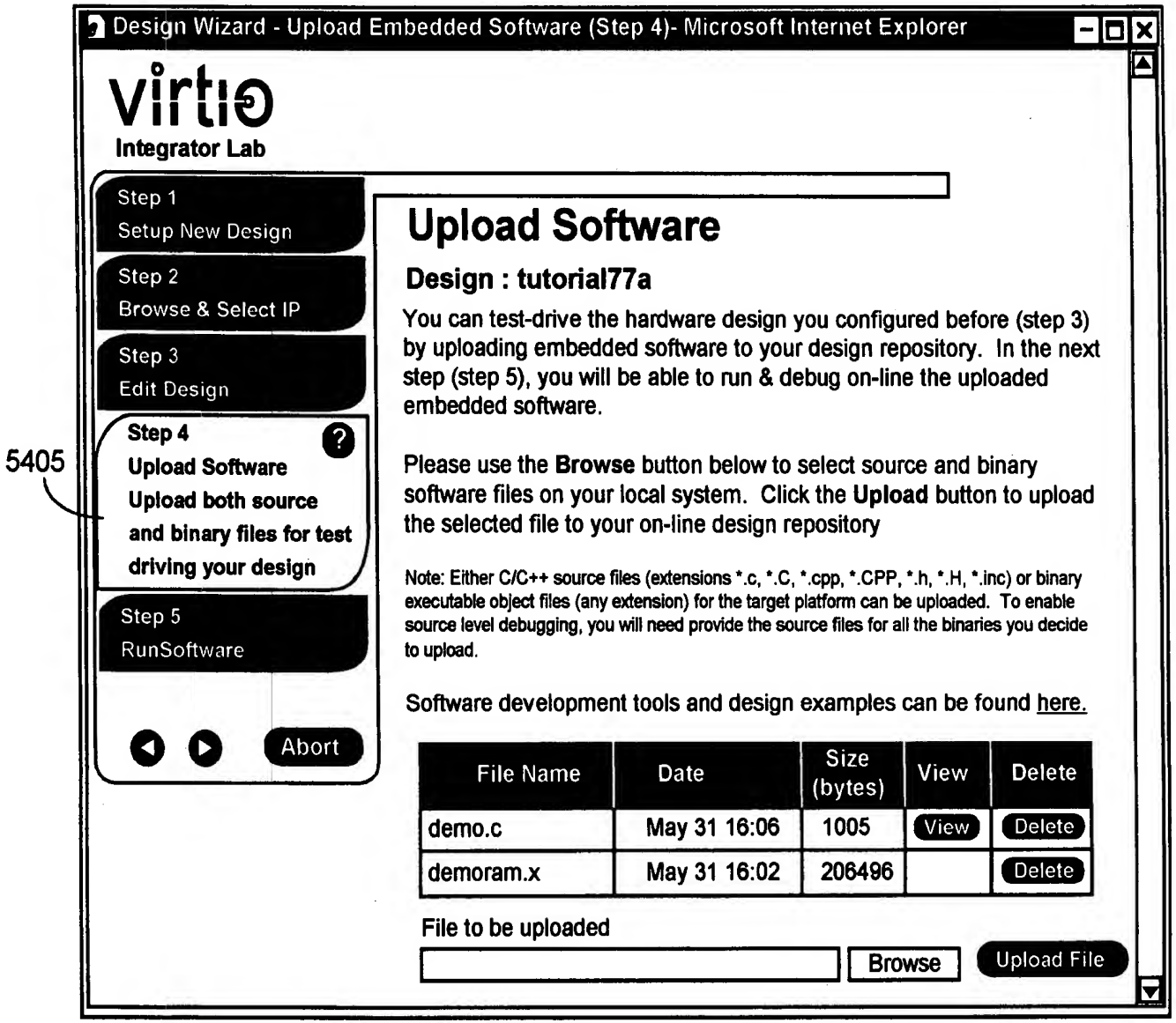


Figure 54

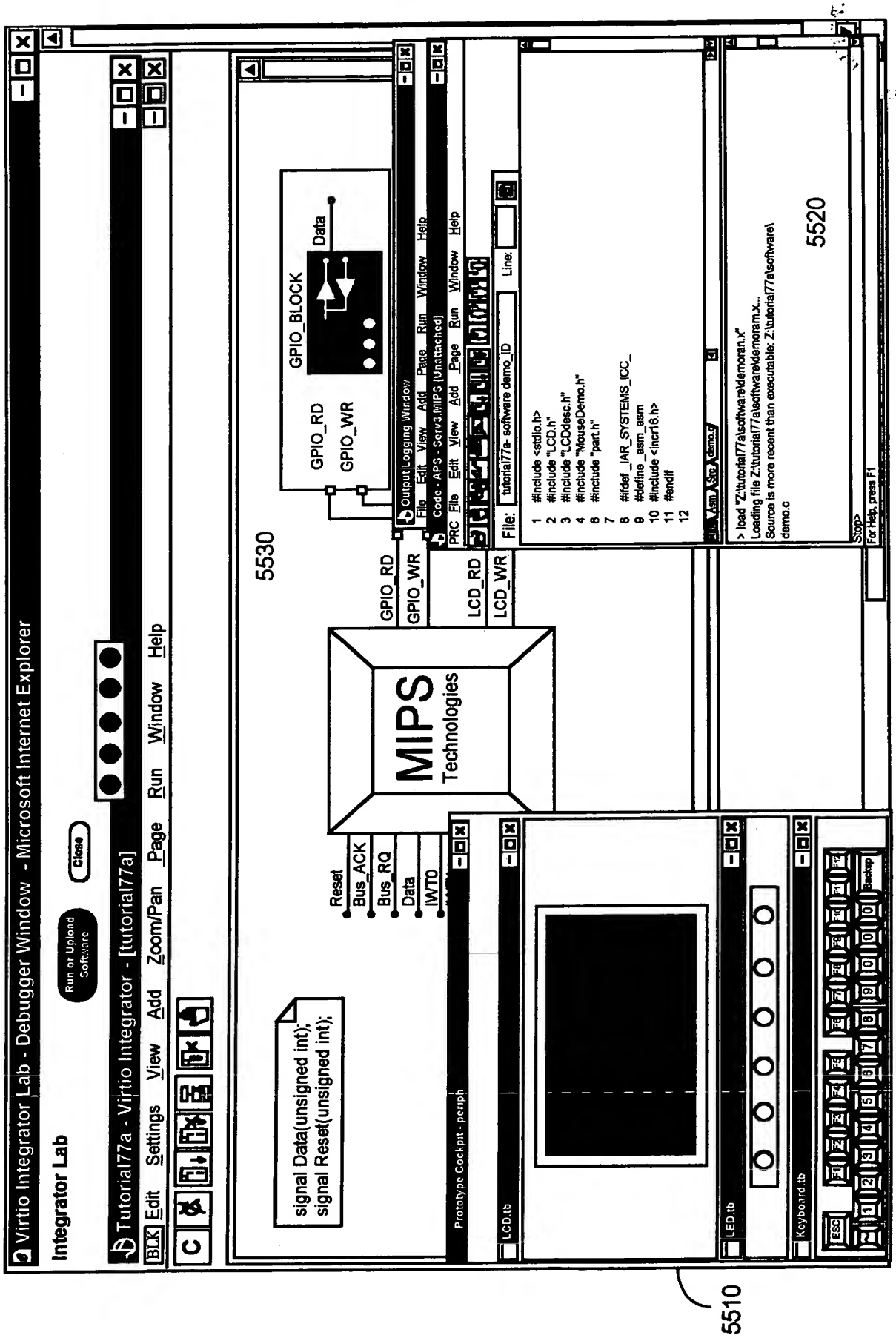

Virtio Integrator Lab - Debugger Window - Microsoft Internet Explorer
Integrator Lab
Run or Upload Software
Close
Tutorial77a - Virtio Integrator - [tutorial77a]
BLK Edit Settings View Add Zoom/Pan Page Run Window Help
5530
GPIO_BLOCK
Data
GPIO_RD
GPIO_WR
Output Logging Window
Code - APS - Serv3.mIPS [Unattached]
File Edit View Add Page Run Window Help
PRC File Edit View Add Page Run Window Help
File: tutorial77a- software demo_ID
Line:
1 #include <stdio.h>
2 #include "LCD.h"
3 #include "LCDdesc.h"
4 #include "MouseDemo.h"
6 #include "part.h"
7
8 #ifdef __IAR_SYSTEMS_ICC__
9 #define _asm_asm
10 #include <incr16.h>
11 #endif
12
GPIO_RD
GPIO_WR
LCD_RD
LCD_WR
MIPS Technologies
Reset
Bus_ACK
Bus_RQ
Data
IWTO
signal Data(unsigned int);
signal Reset(unsigned int);
Prototype Cockpit - periph
LCD.tb
LED.tb
Keyboard.tb
> load "Z:\tutorial77a\software\demoram.x"
Loading file Z:\tutorial77a\software\demoram.x...
Source is more recent than executable: Z:\tutorial77a\software\demo.c
Stop>
For Help, press F1
5520
5510

Figure 55